



Media Fact Sheet

Embedded Instrumentation Comes in Many Shapes, Sizes and Flavors

The names vary, but they're all embedded instruments

May 13, 2008 – Instrumentation is being embedded in chips, on circuit boards and in systems, but, broadly speaking, it is intended for a certain set of applications: design validation, test and debug. Despite the variety of names that it goes by, it's all embedded instrumentation in the end.

The following are some of the aspects of embedded instrumentation as it is being manifested in the electronics industry today.

- **On-Chip Core Instrumentation**

Established chip packaging techniques like system-on-a-chip (SOC) as well as newer techniques such as system-in-package (SiP), package-in-package (PiP) and package-on-package (PoP) are wrecking havoc on older, probe-based methods of design validation, test and debug. In many cases, many of the internal nodes on SOCs, SiPs, PiPs or PoPs are not even accessible to the bonding pad that links the chip to the trace on the circuit board. In addition, signal voltages have shrunk to extremely low levels and noise tolerances have become negligible. To overcome these and other issues, instrumentation is being embedded into the cores of CPUs and other digital chips. Some predict analog devices with embedded instrumentation are soon to follow. To date, on-chip core instrumentation has been applied mostly in chip-level debug applications, but this is expanding rather quickly into other areas such as verification applications.

- **Boundary Scan**

Since it was first defined in the mid-1990s, boundary scan (IEEE 1149.1/JTAG) test has presupposed the embedding of a test infrastructure into chips and onto circuit boards. Follow-on standards that depend upon the 1149.1 standard, such as IEEE 1149.6 for high-speed serial differential buses, likewise rely upon this embedded test infrastructure.

- **Internal JTAG**

A new standard, the IEEE P1687 Internal JTAG (IJTAG) standard, is currently being developed to control, manage, schedule, analyze and access the instrumentation that is being embedded at the core level of chips. Again, the IJTAG standard will rely upon the boundary scan embedded infrastructure in chips and on boards.

- **CPU Emulation**

True CPU emulation – that which can be deployed to perform functional and structural test and diagnostics – is an embedded instrumentation technology in the sense that it takes control of the CPU core and executes test routines on chips and interconnects through the processor. CPU emulation can be accomplished through a processor’s JTAG-based debug port.

- **Device Monitors**

Many semiconductor companies are embedding what they call device monitors into their chips. These are actually embedded instruments which monitor voltages, temperature and other parameters. For example, Maxim has introduced a family of power management chips which features monitoring instrumentation so that the devices can monitor, sequence, track and margin multiple system voltages, adjusting voltages according to pre-programmed limits and storing fault data for further analysis.

- **SERDES (serializer/deserializer) Instrumentation**

High-speed serial buses and chip-to-chip interconnects are very sensitive to electrical noise and distortion. In fact, placing a physical probe on a bus like PCI Express, QuickPath Interconnect (QPI) architecture, Fibre Channel and others only introduces impedance anomalies on the bus, rendering any probe-based validation or test technology practically useless. Several chip and EDA companies are coping with this situation by incorporating embedded instrumentation into high-speed SERDES receiver blocks. These instruments can perform several functions, such as gathering data to plot eye diagrams or to calculate bit error rates.

- **Embedded Test**

Embedded test solutions at the chip level allow integrated circuit designers to embed test functionality into a semiconductor design. This on-chip built-in test functionality is then used during semiconductor production test and throughout the useful life of the chip to reduce device field returns and test costs, accelerating silicon bring-up times and shortening both time to market and time to yield.

- **Post-silicon validation IP**

Focused mostly on SoC validation, debug, and in-system bring-up, post-silicon validation techniques allow design teams to insert reconfigurable instrumentation into their devices, pre-silicon, in order to observe, discover, and diagnose at-speed, in-silicon functional behavior. Physical device validation and debug is the most expensive and unpredictable stage of design implementation. Embedded instruments provide on-chip visibility, which leads to dramatically lower development and integration costs.

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