



A Whitepaper:

**Lead-free assembly shifts test
methods toward boundary scan**

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Table of Contents

Executive Summary	Page 2
Eliminating Harmful Materials	Page 3
Replacement Solder Coumpounds	Page 3
Possible effects of lead-free solder on test	Page 4
Affecting ICT fixturing	Page 4
Boundary scan as an alternative	Page 5

Figures:

Table 1: Melting points of various solder compounds	Page 3
Table 2: The short-term effects of lead-free solder on board test	Page 5

Appendices:

Appendix 1: Traditional Soldering Techniques	Page 6
Appendix 2: Tin Whiskers	Page 7
Appendix 3: Board Flex and μ Strain.	Page 7

Executive Summary

Worldwide the move is on to eliminate pollution-causing lead from the printed circuit board manufacturing process. Already the European Union (EU) has banned lead from all electronic products as of July 2006. Japan followed suit soon thereafter. The US might not be far behind. The effects of ‘getting the lead out’ on electronic test and the use of JTAG test techniques will be far reaching.

Eliminating Harmful Materials

The toxic and harmful effects of lead on the environment have been well documented. As a result, several regions are attempting to eliminate lead-based solder entirely from electronics manufacturing. The European Community (EC) started the trend in the late 1990s with its Waste Electrical and Electronic Equipment (WEEE) and Restrictions of Hazardous Substances (RoHS) initiatives. WEEE dictates that lead solder will be banned from all electronic consumer products sold in Europe by July 1, 2006.

Japan has supported the movement toward lead-free solder and the US, if it wishes to export electronic products to Europe, must conform as well. The North American Electronics Manufacturers Initiative (NEMI) (www.nemi.org) is analyzing the ramifications of lead-free solder.

(For background information on traditional soldering techniques, see Appendix 1: Traditional Soldering Techniques.)

Solders composed of tin and lead have been used for at least 50 years. The most common solder is 63 percent tin and 37 percent lead. Different ratios of tin to lead will affect the melting point of the solder.

Sn-Pb ratios	Melting Point
40/60	230°C
50/50	214°C
60/40	190°C
63/37	183°C
95/5	224°C


 Most common

Table 1: Melting points of various solder compounds

The move to lead-free solder has prompted two questions: what will replace tin/lead solder? And, what effects will the replacement solder have on manufacturing and test processes?

Replacement Solder Compounds

The jury is still out but two alternative solder compounds seem to be emerging, a tin/copper/silver solder and another made up of tin/copper/nickel. For both compounds, the melting point is around 230/240°C, considerably higher than the melting point for tin/lead solders. Actual reflow temperatures peak at 220°C for tin/lead and 260°C for tin/copper/silver. The higher oven temperature required by the replacement solders causes concern among board manufacturers and board test engineers.

Higher soldering temperatures would necessitate higher-temperature components on the boards and high-temperature devices have shorter shelf lives. Fortunately, tests so far on

the higher temperature soldering process do not indicate any internal damage such as internal bond wires lifting, but manufacturers are concerned about board warping, the effect of higher temperatures on heat sinks which act as heat reservoirs, tombstoning and 'tin whiskers.' When pure tin bonds a device to a board, very thin strands or whiskers of tin can spread out at the bond boundary. These whiskers can eventually cause shorting to other connections, either by migration or by breaking off. Adding lead to tin reduces or removes the problem.

For more information on tin whiskers, see Appendix 2: Tin Whiskers.

Silver can also cause problems for electronic manufacturers. In a polluted environment such as an industrial setting, sulphur and chlorine compounds may be present. These react with silver to form a friable (crumbly) layer on the silver. This layer is most likely a silver chloride compound. It has no effect on the conductivity of the silver but it is friable and can break off the surface and contaminate an instrument or electronic system. Because silver chloride is conductive, it can cause shorts when it settles on or is close to interconnects.

Possible effects of lead-free solder on test

Lead-free solder will have several effects on current test techniques. For example, the appearance and geometry of lead-free solder joints will be different from tin/lead solder joints. This may affect manual inspection, AOI or AXI test techniques, although at least one AXI supplier, Agilent Technologies, claims that their 5DX AXI system will be affected very little by lead-free solder.

Another concern arises during board re-work where soldering irons must be at very high temperatures of over 300°C to work with lead-free solder. These high temperatures can damage components on the board that is being re-worked. In addition, intermittent opens can be caused by an oxidation that forms between the pad on the board and the tin/copper/nickel solder.

Affecting ICT fixturing

Lead-free solder may also cause problems for ICT test processes because the lead-free solders are harder to penetrate with the tip of a nail probe. At a time when most manufactures are trying to reduce the force placed on printed circuit boards, more force per nail may be needed to test lead-free solder joints. This would add to the parts-per-million of 'µStrain' placed on the board by the ICT system, shortening the useful life of the nail probe. Currently, nails probe at 6 oz of force on cleaned boards or 8 oz of force on non-cleaned boards. The figure for non-cleaned boards with lead-free solder may have to rise to 10 oz but there is considerable resistance within the industry to anything greater than 8 oz of pressure.

For more information about board flex and µStrain requirements, see Appendix 3: Board Flex and µStrain.

The outcome of this situation may be the following:

- More robust and more costly nails may be required.
- Larger target test pads may be needed for the more robust nails, taking up more, not less, board real estate.
- Multi-prong nail tips could be used, but this would be more expensive than single prong tips.

Boundary scan as an alternative

The transition to lead-free solder could be facilitated by an increased use of JTAG test. Because boundary scan does not require physical access, it does not place any added strain or stress on the board under test. And since it complements ICT processes, any increase in the deployment of boundary scan would reduce the number of test points and nail probes needed for ICT procedures. Given the increasing expense of nails that are strong and durable enough to test lead-free solder joints, any reduction in the number of probes deployed in an ICT fixture would reduce the cost of test significantly.

Summary of major change	Impact on board test based on physical touch i.e. ICT, MDA or FPT	Alternative solution
Introduction of lead-free solder.	Higher assembly temperatures "Tin whiskers" Harder to penetrate test pads Increased risk of board flex More expensive nails with shorter useful life	Greater use of 1149.1 boundary scan to determine the presence of opens and shorts and to reduce/remove the expense of higher-cost fixturing and reduce/ remove the possibility of flexing. AXI still works as well.

Table 2: Summary: The short-term effects of lead-free solder on board test

Bibliography

- [1] Sutton, "Look ahead to the next decade of board test", T&MW, 10/1/1999, www.tmworld.com
- [2] Nelson, "Getting the lead out goes slowly", T&MW, 10/1/2000, www.tmworld.com
- [3] "Tin whiskers", NEMI User group Interim report, June 2003-11-27 www.nemi.org
- [4] Smith, "The impact of Pb-free solder on PCB test and inspection", Teradyne webinar, 3 March 2004, www.teradyne.com

Useful web sites

- [1] www.npl.co.uk Code of practice covering lead-free issues.
- [2] www.lead-free.org Advice of switching to lead-free solder.
- [3] www.envirowise.gov.uk Background on WEEE and RoHS

Appendix 1

Traditional soldering techniques

Traditional solder is an alloy of Tin (Sn) and Lead (Pb). Lead is added to the tin for two reasons: to reduce the melting point and to reduce the risk of “tin whiskers.”

Solder techniques include wave soldering where the board with components passes over a wave of molten solder and reflow soldering where the solder is printed onto the board interconnects and then heated in an oven to melt and bond with the solder balls on a ball grid array package, for example. The soldering process is made easier by the use of a solder flux, which cleans the solder contacts before reflow and prevents oxidation as the solder heats up and becomes molten. Most solder fluxes are a mix of alcohol and rosin (a resin extract from pine trees). Flux can be pre-applied or built into the solder.

With ball grid array packages (BGAs), solder balls are attached to pads on the bottom of the device package. Typically, the pads are spaced 1.27 mm (50 mils) apart and the balls measure 0.76/0.635 mm (25/30 mil) in diameter.

Typical solder flow problems include voids (high-Z joint), cold solder (solder not properly molten before bonding takes place, resulting in resistive joints), poor solder adhesion possibly caused by partial oxidation or by poor pre-solder wetting, full opens (no contact) and solder-to-solder shorts.

Solder defects such as insufficient solder, poor wetting and missing solder balls on power and ground pins are more easily found by AXI techniques rather than with AOI or ICT.

Appendix 2

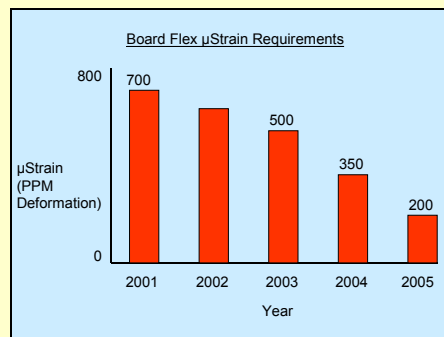
Tin whiskers?

Tin plating generally makes metals more solderable. Tin is a good electrical conductor and also offers corrosion protection. However, along with the benefits of tin plating comes a phenomenon known in the electronics industry as 'tin whiskers.' A tin whisker is a single crystal of tin which grows spontaneously from the plated surface. Manufacturers who prefer the use of tin over lead plating can encounter problems with the interconnections on a board. As tin whiskers grow, they can cause electrical shorts and/or they can flake off, causing physical damage. Tin whiskers are typically no more than a few millimeters long, but even this is enough to cause considerable problems. Many industries using tin plating have reported problems with tin whiskers. In fact, the aerospace industry has experienced the loss of billions of dollars in satellite damage due to this phenomenon.

For more information: <http://www accuratescrew.com/Latest-Tech-Tip.aspx>

Appendix 3

Board Flex and μ Strain



The physical deformation of a board under pressure from a bed-of-nails (sometimes called board flex) is measured in parts per million (ppm) of μ Strain units of deformation. The recommendation of a major board manufacturer is to reduce μ Strain forces from the current 2003 level of 500 ppm to a lower level of 200 ppm by the year 2005, a reduction of 60 percent.

Another major systems company currently is experiencing 600 ppm on a pocket PC board with approximately 700 nails on the ICT fixture. For quality reasons, this is considered too high. In addition, it prevents the testing of two boards at once, limiting the throughput of the manufacturing test process.