



ASSET InterTech Press Backgrounder

*Driving embedded instrumentation for chip
characterization, debug and test, and circuit
board validation, debug and test*

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ASSET: Driving Embedded Instrumentation

ASSET InterTech is a leading supplier of embedded instrumentation tools for validation, test and debug tools for chips, circuit boards and systems. The company's ScanWorks® platform for embedded instrumentation currently supports several test technologies, including boundary scan test, processor-controlled test (PCT) and Intel®'s proprietary embedded instrumentation technology, Interconnect Built-In Self Test (IBIST).

The ScanWorks® platform performs a broad spectrum of tasks. Most notably:

- The ScanWorks platform was the first and is still the only system with tools to access and manage the execution of Intel®'s embedded instrumentation technology, IBIST.
- In non-intrusive board test (NBT) applications, the ScanWorks platform is the only test system that can deploy multiple test technologies – namely, boundary scan, PCT and IBIST – to assert software-driven tests on circuit boards, reducing test costs significantly over hardware-intensive intrusive test technologies while achieving comprehensive test coverage. These same technologies can be implemented in board validation applications as well.
- ScanWorks is the only test platform that will work in concert with Intel's IBIST to validate and test designs featuring high-speed serial buses like PCI Express and QuickPath Interconnect (QPI).
- ScanWorks was one of the first boundary scan (IEEE 1149.1/JTAG) systems capable of automatically developing structural tests, applying those tests to circuit boards, and diagnosing faults and failures.
- With its PCT technology, ScanWorks asserts structural and functional test and diagnostic routines through the processor to other devices and to other nodes on circuit boards
- ScanWorks' PCT technology supports a wide range of Intel processors, including some of that company's most advanced devices such as the Atom™ and the Xeon® Processor 5500 Series (Nehalem), as well as many non-Intel processors such as ARM, PowerPC and others.

What's New from ASSET

At the International Test Conference (ITC) in November of 2009, ASSET announced an agreement with SiliconAid Solutions, Inc. of Austin, Texas, whereby that firm's chip debugger tool will be integrated into the ScanWorks platform for embedded instrumentation and ASSET will re-sell SiliconAid's tools for the insertion and verification of IEEE P1687 Internal JTAG (IJTAG) into chips. SiliconAid is a supplier of electronic design automation (EDA) and testability tools. IEEE P1687 IJTAG is being developed as an industry standard interface to embedded instrumentation in chips so that these instruments can be accessed, automated and analyzed in a uniform manner no matter the source of the embedded instrumentation intellectual property (IP). The relationship between ASSET and SiliconAid announced at ITC 2009 will also involve joint marketing and sales activities by the two companies.

Test and Validation Technologies on ScanWorks

ScanWorks is an open software platform for embedded instrumentation tools. It engages the test and measurement embedded instrumentation in chips and on circuit boards through several test and validation technologies. See Figure 1 below.



Figure 1

Intel® IBIST

IBIST (Interconnect Built-In Self Test) is an embedded instrumentation technology Intel has been inserting into its next-generation chips and chipsets to more effectively validate high-speed serial buses on circuit boards and lower the overall cost of board test. The ScanWorks tools for IBIST include pattern generation and checking, bit error rate test (BERT) and margining. The IBIST technology has been adopted by other semiconductor and intellectual property (IP) companies such as Avago.

Processor-Controlled Test (PCT)

PCT takes advantage of the JTAG port or, in the case of Intel processors, the debug port on processors to deliver test and diagnostic code, which is run by the processor at full operational speeds. These routines include bus tests, memory tests and I/O tests. PCT

takes control of the processor at reset and instructs it to write appropriate test data to each addressable device, verifying or diagnosing each device and its associated interconnects and buses.

Boundary Scan

Since its ratification more than a decade ago, the IEEE 1149.1 Boundary-Scan Standard has evolved from a non-intrusive hardware test capability for circuit boards to a board- and system-level infrastructure technology that provides the basis for much more than simple interconnect test. Boundary scan has emerged and will continue to evolve in the future as a foundational technology for a host of complementary capabilities, such as IEEE 1149.6 high-speed AC-coupled test, Intel® IBIST, IEEE P1687 JTAG, processor-controlled test (PCT), IEEE 1532 in-system configuration (ISC) of programmable logic, in-system programming (ISP) of flash memory, IEEE 1149.4 analog test and much more.

ASSET's Beginning

ASSET InterTech began as a business unit of Texas Instruments (TI). In July of 1995, TI's ASSET product family and related business were acquired by ASSET InterTech, Inc., which was founded by the team that had designed, developed and marketed the ASSET product as a part of TI for the previous six years. ASSET InterTech has an installed base of more than 5,000 systems worldwide in hundreds of organizations. Among its customers are prominent companies such as Cisco, Ericsson, Motorola, Alcatel-Lucent, Tellabs, Huawei, Raytheon, Rockwell, Lockheed Martin, BAE, ITT, Northrop Grumman, GE Aviation and others.

Driving Embedded Instrumentation

At a time when chips are becoming much more complex every day, the data transfer rates and sensitivities of chip-to-chip buses on circuit boards are escalating exponentially. Many of today's tools simply cannot adequately validate or test designs with leading edge chips and high-speed serial buses, like PCI Express, Quick Path Interconnect (QPI) and others. As a result, many organizations are opting to embed certain validation, test and debug functionality at the chip level in the form of embedded instrumentation.

The ScanWorks platform brings to chip and board validation and test applications an established, easy-to-use, well understood way of accessing, controlling and managing chip and board level constructs. ScanWorks provides these capabilities in an intuitive graphical user interface.

New Embedded Instrumentation Standards

Several new standards that relate to embedded instrumentation are being developed or will soon be ratified. These include the IEEE P1687 Internal JTAG (IJTAG) standard and the IEEE 1149.7 standard that adds test enhancements to the original IEEE 1149.1 boundary scan standard and defines a compact two-wire boundary-scan Test Access Port

(TAP) interface. ASSET occupies leadership positions on the working groups that are developing both of these standards.

- **IEEE P1687 IJTAG (Internal JTAG)**

The IJTAG working group has issued a draft hardware architecture that defines an embedded instrument as any embedded logic within a chip for test, debug-diagnostic, configuration or operational purposes, and which can be accessed and operated from within the IJTAG framework. Examples of IJTAG instruments are scan architectures, memory BIST engines (Built-In Self Test), logic BIST engines, clock-controllers, data capture buffers, embedded logic analyzers and many others which will be developed in the future. The intent of the IJTAG working group is to develop a standard interface to embedded instrumentation no matter the source of the instrument. Such a standard would encourage the development of open tools to streamline the access, automation and analysis of embedded instrumentation. ASSET's Al Crouch, chief technologist-core instrumentation, is the co-chairman of the IJTAG working group.

- **IEEE 1149.7 compact boundary scan standard**

A complementary and enhanced derivative of IEEE 1149.1 (the original boundary-scan or JTAG standard), the IEEE 1149.7 standard is completely backward compatible with the extensive base of embedded IEEE 1149.1 technology. 1149.7 certainly can and will be deployed as a narrow (two-wire) interface in some applications, but the standard also allows for wide (four/five-wire) implementation as well. Architectural enhancements have been made to the 1149.7 specification to accommodate the testing of three-dimensional (3D) chips in multi-die packages. The 1149.7 standard offers the advantage that it can be deployed effectively using through-silicon vias. ASSET's Adam Ley, chief technologist-boundary scan, is a founding member of the 1149.7 working group and the chief author of the standard's test content.

Strategic Relationships

ASSET has established strategic marketing and development relationships with several prominent companies, including Intel®, Cadence, Mentor and Synopsys.

Since 2004, Intel and ASSET have worked closely together on support tools for Intel's next-generation embedded instrumentation technology, Intel IBIST. ScanWorks is the only boundary scan system to support Intel IBIST.

ASSET and Cadence are working together to integrate ScanWorks into the Cadence Encounter Digital IC Design flow. This integration will enable design and test engineers to embed instrumentation tools into complex system-on-chip (SoC) and system-in-package (SiP) devices.

In addition, ASSET is a member of Synopsys' In-Sync program. Synopsys has supplied ASSET engineers with products to synthesize and verify chip-level DFT-related

structures. ASSET has verified interoperability between ScanWorks and Synopsys' TetraMAX® Automatic Test Pattern Generator (ATPG), TetraMAX DSMTest, DFT MAX compression, BSD Compiler boundary scan, and VCS® MX mixed Verilog and VHDL simulator.

Moreover, ASSET is a member of Mentor Graphics' OpenDoor Program in order to ensure toolset interoperability for embedded instrumentation applications. Through this program, ASSET and Mentor will enable the exchange of data between Mentor's chip-level inserted design-for-test (DFT) structures, such as the JTAG infrastructure, and ASSET's ScanWorks platform for embedded instrumentation.

Management Team and Board of Directors

Management Team

Glenn Woppman, President and CEO

Prior to being named president and CEO in 1995 when ASSET InterTech became an independent company, Mr. Woppman was product manager for the ASSET business unit within TI. He was responsible for all business functions relating to ASSET, including sales, marketing, R&D and finance. Mr. Woppman has managed 30 percent annual growth for the group and has helped to establish the ASSET ScanWorks product family as a leading technology in the test industry. He has an MBA from Southern Methodist University and a BSIE from the University of South Florida.

Gerry Morgan, Vice President, Product Development

Mr. Morgan has more than 20 years of experience in the test industry. He has worked for Fairchild Semiconductor, GenRad®, where he led development projects such as the Encompass software that runs on the GENEVA Test System, and Brooks Automation. He holds an MBA from Northeastern University, and BS and ME degrees in Electrical Engineering from the University of Maine.

Alan Sguigna, Vice President of Sales and Marketing

Mr. Sguigna has more than 20 years of experience in senior-level general management, marketing, engineering, sales, manufacturing, finance and customer service positions. Before joining ASSET, he worked in the telecom industry. He has had profit and loss responsibility for a \$150 million division of Spirent Communications, a supplier of test products and services. Prior to his tenure with Spirent, Mr. Sguigna also served in business development positions with Nortel Networks, overseeing the growth of its voice over Internet protocol (VoIP) products.

Adam Ley, Chief Technologist-Boundary Scan

Mr. Ley is responsible for plotting the direction of ASSET's industry-leading boundary scan technology. Additionally, he participates in various industry bodies, including the IEEE 1149.1 working group on boundary scan and the IEEE 1149.6 committee that is developing test methodologies for high-speed serial AC-coupled nets. He has been involved in boundary-scan technology since 1991 and was a key technical leader for

Texas Instrument's Logic Products division's efforts to develop and bring to market its line of boundary-scan bus interface and scan support products. He holds a BSEE degree from Oklahoma State University.

Al Crouch, Chief Technologist-Core Instrumentation

Al Crouch is a Senior Member of the IEEE. He was formerly chief scientist and director of research and development at Inovys Corp. of Pleasanton, Calif., and Verigy Ltd. of Cupertino, Calif. Mr. Crouch has served as the vice chairman of the IEEE P1687 IJTAG working group that is developing the IJTAG standard and has contributed significantly to the hardware architecture definition. Over the last 20 years, he has accumulated vast experience in chip design-for-test at both Freescale Semiconductor (formerly Motorola) and Texas Instruments. Mr. Crouch has filed for more than 30 patents and been granted 15.

Tim Caffee, Vice President of Design Validation

Mr. Caffee's business unit is responsible for bringing new tools to market that will validate the design of next-generation products. Previous to this position, he played a key role in new business development, facilitating global deployment of boundary-scan tools and managing key customer accounts. He was a founder of ASSET and has spent 15 years working with boundary-scan tools. Prior to ASSET, he spent several years at Texas Instruments in the defense business unit. Mr. Caffee obtained B.S. degrees in Mathematics and Computer Science at Old Dominion University.

Arden Bjerkeli, Director of Customer Applications Support

As director of customer applications support, Mr. Bjerkeli manages a group of engineers that provides pre- and post-sales support, customer-driven maintenance and other services, and customer training. Prior to joining ASSET, He held various engineering management positions for Compaq Computer Corporation for more than 16 years. At Compaq, he managed several engineering groups that were responsible for developing and testing new desktop computer and server products. In addition, he served in several testability research and development positions. He has a bachelor's degree in Electrical Engineering from the University of Houston.

Brent Troxel, Director of Financial Control, Analysis and Operations

Mr. Troxel is responsible for monitoring all of ASSET's financial information and compiling the company's financial analysis and reports. He came to ASSET from TXP Corporation, where he was controller and a member of the senior management team. Previous to that he served in accounting positions at Verizon Communications, GTE Corp., and Andersen Consulting. He has an MBA from the University of Dallas and a Bachelor's Degree in Accounting from Indiana University.

Board of Directors

Glenn Woppman, President and CEO

See biographical information under Management Team above.

Bill Drobish

Mr. Drobish has over 30 years of executive and management experience in the high tech and software industry. He was one of the three founders of Silicon Systems and helped manage that company as its sales grew to more than \$100 million. Mr. Drobish has been involved to varying degrees with several other start-up electronics companies. He currently has served on the board of TMA, Microsim (P-Spice), Kofax Image Products and many others. He has an electrical engineering degree from Purdue University.

Tim Dehne

Over a career stretching more than 21 years at National Instruments, Austin, TX, Mr. Dehne led global marketing, and research and development at the company that had \$824 million in revenues in 2008. During his tenure at NI, Mr. Dehne served as vice president of strategic marketing, vice president of marketing, vice president of research and development, and senior vice president of research and development. In addition to serving on the ASSET board of directors he is currently the vice president of systems and research and development for Luminex Corporation, Austin, TX,

Andy Mindlin

Mr. Mindlin of Corona del Mar, Calif., is a management consultant and president of RealWorld Marketing, Inc., which provides marketing and general management assistance to high technology and high-growth firms. Mr. Mindlin has over 18 years of experience in product development, marketing, general management and sales. He previously held marketing positions with Proctor & Gamble and Richardson-Vicks. Mr. Mindlin is a Phi Beta Kappa graduate of Vanderbilt University.

Anthony J. LeVecchio

Mr. LeVecchio is the president and owner of The James Group, Inc., a business support and development company in Dallas. At various times during his career, Mr. LeVecchio has acted as both an interim chief financial officer and as a financial oversight executive to assist companies with financial planning, cash management, internal controls, strategic and operating plans, negotiated settlements and stock structures. He has served as CFO of VHA Southwest and Phillips Information Systems. He also worked for Exxon Office Systems and Xerox Corporation. He has a BA in Economics and an MBA in Finance from Rollins College.

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