



Driving Embedded Instrumentation

## **ASSET InterTech Press Backgrounder**

*Driving embedded instrumentation for chip,  
board and system validation, debug and test*

ASSET® InterTech, Inc.  
2201 North Central Expressway, Suite 105  
Richardson, TX 75080  
(972) 437-2800  
[www.asset-intertech.com](http://www.asset-intertech.com)

**Press Contact:**  
Bob Greenfield  
G&A PR  
(972) 254-2887  
Bob.greenfield@verizon.net

## **ASSET: Driving Embedded Instrumentation**

ASSET InterTech is a leading supplier of embedded instrumentation tools for the validation, test and debug of chips, circuit boards and systems. The company's ScanWorks® platform for embedded instruments currently supports several test technologies, including the industry's first tools for the IEEE 1687 Internal JTAG (IJTAG) standard for embedded instruments (announced Nov. 2, 2010). Other technologies supported by ScanWorks include boundary scan test (IEEE 1149.1 or JTAG), processor-controlled test (PCT) and Intel®'s proprietary embedded instrumentation technology, Interconnect Built-In Self Test (IBIST).

The ScanWorks® platform performs a broad spectrum of tasks. Most notably:

- Following a seven-year collaboration with Intel, ScanWorks is the first third-party validation and debug tool for designs based on the 22 nm Intel® microarchitecture codename Ivy Bridge
- ScanWorks is also the first test toolkit for Intel's new second generation Core™ (codename Sandy Bridge) processors (i3, i5 and i7)
- The ScanWorks platform automates the development of validation and test routines based on the IEEE P1687 IJTAG embedded instrumentation standard
- ScanWorks is the only system with tools to access and manage the execution of Intel®'s embedded instrumentation technology, IBIST.
- In non-intrusive board test (NBT) applications, the ScanWorks platform is the only test system that can deploy multiple test technologies – namely: IJTAG-based instruments, boundary scan, PCT and IBIST – to assert software-driven tests on circuit boards. This reduces test costs significantly over hardware-intensive intrusive test technologies while achieving comprehensive test coverage. These same technologies can be implemented in board validation applications as well.
- ScanWorks is the only test platform that works in concert with Intel's IBIST to validate and test designs featuring high-speed serial buses like PCI Express, QuickPath Interconnect (QPI) and others.
- ScanWorks was one of the first boundary scan (IEEE 1149.1/JTAG) systems capable of automatically developing structural tests, applying those tests to circuit boards, and diagnosing faults and failures.
- With its PCT technology, ScanWorks asserts structural and functional test and diagnostic routines through the processor to other devices and nodes on circuit boards
- ScanWorks' PCT technology supports a wide range of Intel processors, including some of that company's most advanced devices such as the Atom™ and the Xeon® Processors 7500 and 5500 Series (based on the Nehalem microarchitecture), as well as many non-Intel processors such as ARM cores, PowerPC processors and others.

## What's New from ASSET

At Embedded 2011, ASSET announced that ScanWorks is the first third-party validation and debug platform with tools for designs based on the Intel® microarchitecture codename Ivy Bridge (22nm) for the desktop and mobile marketplaces. Relative to Ivy Bridge designs, ScanWorks is a high-level diagnostic tool that can graphically visualize and display validation and debug information down to the level of an individual bit or a specific lane on a high-speed serial bus. The buses that can be validated include the DDR3, PCI Express Graphics (PEG) and Direct Media Interface (DMI) buses.

In addition, ASSET recently announced (Feb. 15, 2011) that ScanWorks is the first test tool for Intel's new second generation Core i3, i5 and i7 processors (codename Sandy Bridge). As a result, manufacturers are able to perform structural and functional tests at processor speeds on circuit boards with 2nd generation Core processors intended for mobile and desktop applications.

For more information on these announcements, go to the ASSET press room at: <http://www.asset-intertech.com/news.html>

## Test and Validation Technologies on ScanWorks

The software-driven ScanWorks is an open tools platform for embedded instruments. It engages the test and measurement embedded instrumentation in chips and on circuit boards through several test and validation technologies. See Figure 1 below.



Figure 1

The validation, test and debug technologies that operate on the ScanWorks platform are:

### **IJTAG**

The IEEE P1687 IJTAG standard is expected to be ratified during 2011. IJTAG specifies a standard access architecture and protocol for instruments that are embedded into chips. In addition, it defines how these embedded instruments can be accessed and automated, and their output analyzed.

### **Intel® IBIST**

IBIST (Interconnect Built-In Self Test) is an embedded instrumentation technology Intel has been inserting into its next-generation chips and chipsets. IBIST effectively validates and tests high-speed serial buses on circuit boards and lowers the overall cost of board test. The ScanWorks tools for IBIST include pattern generation and checking, bit error rate test (BERT) and margining. The IBIST technology has been adopted by other semiconductor and intellectual property (IP) companies including Avago Technologies.

### **Processor-Controlled Test (PCT)**

PCT takes advantage of a processor's JTAG port or, in the case of Intel processors, the debug port to deliver test and diagnostic code, which is run by the processor at full operational speeds. These routines include bus tests, memory tests and I/O tests. PCT takes control of the processor at reset and instructs it to write appropriate test data to each addressable device, verifying or diagnosing each device and its associated interconnects and buses.

### **Boundary Scan**

Since its ratification more than a decade ago, the IEEE 1149.1 Boundary-Scan Standard has evolved from a non-intrusive hardware test capability for circuit boards to a board- and system-level infrastructure technology that provides the basis for much more than simple interconnect test. Boundary scan has emerged and will continue to evolve in the future as a foundational technology for a host of complementary capabilities, such as IEEE 1149.6 high-speed AC-coupled test, Intel® IBIST, IEEE P1687 IJTAG, processor-controlled test (PCT), IEEE 1532 in-system configuration (ISC) of programmable logic, in-system programming (ISP) of flash memory, IEEE 1149.4 analog test, the enhanced IEEE 1149.7 compact boundary scan for system-on-chip (SoC) validation and test, and much more.

## **ASSET's Beginning**

ASSET InterTech began as a business unit of Texas Instruments (TI). In July of 1995, TI's ASSET product family and related business were acquired by ASSET InterTech, Inc., which was founded by the team that had designed, developed and marketed the ASSET product as a part of TI for the previous six years. ASSET InterTech has an installed base of more than 5,000 systems worldwide in hundreds of organizations. Among its customers are prominent companies such as Cisco, Ericsson, Motorola, Flextronics, Alcatel-Lucent, Tellabs, Huawei, Raytheon, Rockwell, Lockheed Martin, BAE, ITT, Northrop Grumman, GE Aviation and others.

## Driving Embedded Instrumentation

At a time when chips are becoming much more complex every day, the data transfer rates and sensitivities of chip-to-chip buses on circuit boards are escalating exponentially. Many of today's tools simply cannot adequately validate or test designs with leading-edge chips and high-speed serial buses, like PCI Express, Quick Path Interconnect (QPI) and others. As a result, many organizations are opting to embed certain validation, test and debug instruments into chips.

The ScanWorks platform brings to chip and board validation and test applications an established, easy-to-use, well understood way of accessing, controlling and managing chip and board level constructs. ScanWorks provides these capabilities in an intuitive graphical user interface.

## ASSET's Embedded Instrumentation Ecosystem

As the embedded instrumentation market evolves, ASSET continues to assemble a powerful ecosystem featuring manufacturers, ODM/EMS firms, ATE suppliers, chip vendors, logic producers, memory providers, programmable device vendors and EDA suppliers. Essential to the success that will accrue to this web of interrelated organizations is the technology made possible by the IEEE P1687 IJTAG standard. IJTAG capabilities in chips, on circuit boards and in systems will function as the connective tissue that binds together the ecosystem shown below.



As part of its ecosystem strategy, ASSET has established strategic marketing and development relationships with many prominent companies, including Intel®, Flextronics, Cadence, Mentor and Synopsys.

Since 2004, Intel and ASSET have worked closely together on support tools for Intel's next-generation embedded instrumentation technology, Intel IBIST. ScanWorks is the only boundary scan system to support Intel IBIST.

On Nov. 2, 2010, ASSET announced it has partnered with the major electronic manufacturing services (EMS) firm, Flextronics, to accelerate the adoption of the IEEE P1687 IJTAG standard for embedded instruments. One of Flextronics' Centers of Excellence has adopted the ScanWorks IJTAG toolkit and is collaborating with ASSET on its further development.

ASSET and Cadence are working together to integrate ScanWorks into the Cadence Encounter Digital IC Design flow. This integration will enable design and test engineers to embed instrumentation tools into complex system-on-chip (SoC) and system-in-package (SiP) devices.

In addition, ASSET is a member of Synopsys' In-Sync program. Synopsys has supplied ASSET engineers with products to synthesize and verify chip-level DFT-related structures. ASSET has verified interoperability between ScanWorks and Synopsys' TetraMAX® Automatic Test Pattern Generator (ATPG), TetraMAX DSMTest, DFT MAX compression, BSD Compiler boundary scan, and VCS® MX mixed Verilog and VHDL simulator.

Moreover, ASSET is a member of Mentor Graphics' OpenDoor Program in order to ensure toolset interoperability for embedded instrumentation applications. Through this program, ASSET and Mentor will enable the exchange of data between Mentor's chip-level inserted design-for-test (DFT) structures, such as the JTAG infrastructure, and ASSET's ScanWorks platform for embedded instrumentation.

## **Management Team and Board of Directors**

### **Management Team**

#### Glenn Woppman, President and CEO

Prior to being named president and CEO in 1995 when ASSET InterTech became an independent company, Mr. Woppman was product manager for the ASSET business unit within TI. He was responsible for all business functions relating to ASSET, including sales, marketing, R&D and finance. Mr. Woppman has managed 30 percent annual growth for the group and has helped to establish the ASSET ScanWorks product family as a leading technology in the test industry. He has an MBA from Southern Methodist University and a BSIE from the University of South Florida.

#### Gerry Morgan, Vice President, Product Development

Mr. Morgan has more than 20 years of experience in the test industry. He has worked for Fairchild Semiconductor, GenRad®, where he led development projects such as the Encompass software that runs on the GENEVA Test System, and Brooks Automation. He holds an MBA from Northeastern University, and BS and ME degrees in Electrical Engineering from the University of Maine.

#### Alan Sguigna, Vice President of Sales and Marketing

Mr. Sguigna has more than 20 years of experience in senior-level general management, marketing, engineering, sales, manufacturing, finance and customer service positions. Before joining ASSET, he worked in the telecom industry. He has had profit and loss responsibility for a \$150 million division of Spirent Communications, a supplier of test products and services. Prior to his tenure with Spirent, Mr. Sguigna also served in business development positions with Nortel Networks, overseeing the growth of its voice over Internet protocol (VoIP) products.

#### Adam Ley, Chief Technologist-Boundary Scan

Mr. Ley is responsible for plotting the direction of ASSET's industry-leading boundary scan technology. Additionally, he participates in various industry bodies, including the IEEE 1149.1 working group on boundary scan and the IEEE 1149.6 committee that is developing test methodologies for high-speed serial AC-coupled nets. He has been involved in boundary-scan technology since 1991 and was a key technical leader for Texas Instrument's Logic Products division's efforts to develop and bring to market its line of boundary-scan bus interface and scan support products. He holds a BSEE degree from Oklahoma State University.

#### Al Crouch, Chief Technologist-Core Instrumentation

Al Crouch is a Senior Member of the IEEE. He was formerly chief scientist and director of research and development at Inovys Corp. of Pleasanton, Calif., and Verigy Ltd. of Cupertino, Calif. Mr. Crouch has served as the vice chairman of the IEEE P1687 IJTAG working group that is developing the IJTAG standard and has contributed significantly to the hardware architecture definition. Over the last 20 years, he has accumulated vast experience in chip design-for-test at both Freescale Semiconductor (formerly Motorola) and Texas Instruments. Mr. Crouch has filed for more than 30 patents and been granted 15.

Tim Caffee, Vice President of Design Validation

Mr. Caffee's business unit is responsible for bringing new tools to market that will validate the design of next-generation products. Previous to this position, he played a key role in new business development, facilitating global deployment of boundary-scan tools and managing key customer accounts. He was a founder of ASSET and has spent 15 years working with boundary-scan tools. Prior to ASSET, he spent several years at Texas Instruments in the defense business unit. Mr. Caffee obtained B.S. degrees in Mathematics and Computer Science at Old Dominion University.

Arden Bjerkeli, Director of Customer Applications Support

As director of customer applications support, Mr. Bjerkeli manages a group of engineers that provides pre- and post-sales support, customer-driven maintenance and other services, and customer training. Prior to joining ASSET, He held various engineering management positions for Compaq Computer Corporation for more than 16 years. At Compaq, he managed several engineering groups that were responsible for developing and testing new desktop computer and server products. In addition, he served in several testability research and development positions. He has a bachelor's degree in Electrical Engineering from the University of Houston.

Brent Troxel, Director of Financial Control, Analysis and Operations

Mr. Troxel is responsible for monitoring all of ASSET's financial information and compiling the company's financial analysis and reports. He came to ASSET from TXP Corporation, where he was controller and a member of the senior management team. Previous to that he served in accounting positions at Verizon Communications, GTE Corp., and Andersen Consulting. He has an MBA from the University of Dallas and a Bachelor's Degree in Accounting from Indiana University.

**Board of Directors**

Glenn Woppman, President and CEO

See biographical information under Management Team above.

Bill Drobish

Mr. Drobish has over 30 years of executive and management experience in the high tech and software industry. He was one of the three founders of Silicon Systems and helped manage that company as its sales grew to more than \$100 million. Mr. Drobish has been involved to varying degrees with several other start-up electronics companies. He currently has served on the board of TMA, Microsim (P-Spice), Kofax Image Products and many others. He has an electrical engineering degree from Purdue University.

Tim Dehne

Over a career stretching more than 21 years at National Instruments, Austin, TX, Mr. Dehne led global marketing, and research and development at the company that had \$824 million in revenues in 2008. During his tenure at NI, Mr. Dehne served as vice president of strategic marketing, vice president of marketing, vice president of research and development, and senior vice president of research and development. In addition to serving on the ASSET board of

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directors he is currently the vice president of systems and research and development for Luminex Corporation, Austin, TX,

### Andy Mindlin

Mr. Mindlin of Corona del Mar, Calif., is a management consultant and president of RealWorld Marketing, Inc., which provides marketing and general management assistance to high technology and high-growth firms. Mr. Mindlin has over 18 years of experience in product development, marketing, general management and sales. He previously held marketing positions with Proctor & Gamble and Richardson-Vicks. Mr. Mindlin is a Phi Beta Kappa graduate of Vanderbilt University.

### Anthony J. LeVecchio

Mr. LeVecchio is the president and owner of The James Group, Inc., a business support and development company in Dallas. At various times during his career, Mr. LeVecchio has acted as both an interim chief financial officer and as a financial oversight executive to assist companies with financial planning, cash management, internal controls, strategic and operating plans, negotiated settlements and stock structures. He has served as CFO of VHA Southwest and Phillips Information Systems. He also worked for Exxon Office Systems and Xerox Corporation. He has a BA in Economics and an MBA in Finance from Rollins College.

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