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Non-Intrusive Board Test Gains Momentum

It doesn't seem so long ago that dedicated automatic-test-equipment exhibitions required stands of sizeable acreage for the manufacturers showing off their latest products. Semiconductor devices were not so complex, and most were soldered to the circuit board. Moore's Law has moved semiconductor technology on at a rattling pace, and BGA (ball-grid-array) packaging and other techniques have made chip testing a tougher task. Hence the momentum behind non-intrusive testing.

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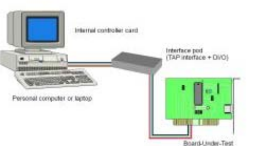

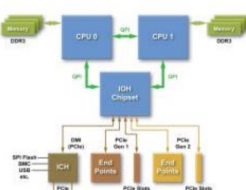

Since its emergence, the electronics industry has mostly relied upon intrusive test technologies based on probes or fixtures, which make physical contact with pins on chips or test pads on circuit boards. Over the last 10 years, the ability of intrusive technologies such as ICT (in-circuit test), flying probe test, oscilloscopes, MDAs (manufacturing-defect analysers) and others has diminished severely. The speed, complexity and geometries of chips and circuit-board designs have progressed beyond the reach of intrusive test technologies. Quite simply, physical access does not and cannot produce the test results it once could when chips were larger and slower, circuit boards were bigger and less complex, and device packaging featured exposed pins large enough to probe.

Now, NBT (non-intrusive board test) is emerging as the prime test solution of the future. Intrusive test systems can be expensive pieces of equipment so, as well as technology, economics has dictated the pace of change. Unlike intrusive technologies, which require large and expensive hardware systems and costly fixtures, non-intrusive technologies are software-driven. NBT gains access to chips and circuit boards via a simple connector on the board. An NBT test station typically consists of a personal computer that is running the test system's software and other tools. Quite often, NBT gains access to the UUT (unit under test) via the IEEE 1149.1 boundary-scan (JTAG) interface, but other technologies could also serve this purpose. An NBT technology applies internal electrical test patterns to the chips and the circuit board. These test patterns exercise the chips and the structures on the circuit board, and the results are observed. To facilitate rapid repair, faults and failures in the electrical continuity or the structural integrity of the board can be further diagnosed to pinpoint their cause and location.

The need for non-intrusive test methodologies has become acute in recent years as chips and circuit-board-design techniques have denied physical access to components. Fine-pitch chips, high-density interconnects, blind and buried vias, BGA chip packaging, multi-die chips, heat sinks, conformal coating and other chip- and board-design issues now quite commonly prevent physical access for electrical testing. Furthermore, for years it has been a standard circuit-board-design practice to insert test pads on the surface of the board. These small contact points provided physical access to the underlying buses for test purposes. Recently, high-speed serial interconnects like PCIe (PCI Express) 2.0 or 3.0, Fibre Channel, 10-Gbps Ethernet, InfiniBand, Intel's QPI (QuickPath Interconnect) and others have become more and more commonplace. Quite simply, placing a metal probe on a test pad on these high-speed serial interconnects introduces signal-integrity anomalies. Specifically, test pads and probes introduce capacitance on the bus that renders any intrusive test measurement unreliable.

Strength in numbers

Because it is software-driven, NBT is able to effectively launch and apply multiple test technologies from a single hardware platform to the same UUT. By doing so, NBT can achieve very high test coverage, recovering all or most of the coverage lost to disappearing physical access and often testing aspects of the design that intrusive technologies could not. For example, an NBT test strategy could include boundary-scan test, emulation-based processor-controlled test and a built-in self test technique such as Intel's IBIST (Interconnect Built-In Self Test). These non-intrusive technologies rely on embedded instrumentation within silicon to deliver test coverage. Embedded instrumentation is defined as IP (intellectual property), either conforming to an industry standard or a proprietary technology within devices; this enables validation, test and debug of chips, boards and systems.

Boundary-scan test

The IEEE 1149.1 Boundary Scan Standard was developed in the mid-1990s because fine-pitch pins on chips could not be probed or the pins were disappearing under the silicon die in BGA packages (Figure 1). Chips conforming to the IEEE 1149.1 standard have several registers that are dedicated to boundary-scan test. Test patterns are applied to a circuit board through a four-wire interface called the Test Access Port. This interface on chips is commonly referred to as the

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"JTAG port", which is derived from the name of the informal working group that began the development of the standard, the Joint Test Action Group. Boundary scan has been widely adopted by the industry. In fact, the original IEEE 1149.1 standard has become the basis for several additional standards, including the IEEE 1149.6 for high-speed AC-coupled interconnects, a newly enhanced version of 1149.1, the 1149.7 standard, and others.

Processor-controlled test

Processor-controlled test is sometimes referred to as functional processor-emulation test. It makes use of the boundary-scan infrastructure on a circuit board and in the chips on the board. As the name "processor-controlled test" implies, control of the board's processor is temporarily handed over to the test platform so that test algorithms can be applied at processor speeds through the I/O pins that connect the chips on the board to the processor. Test patterns are propagated through the processor, and the board's functionality is exercised at operational speeds, detecting and diagnosing any structural faults found on the board. Since it is an at-speed technology, processor-controlled test will detect faults that remain undetected by static test technologies—including many of the intrusive techniques, such as ICT, flying probe and MDA.

Intel Interconnect Built-In Self Test

Intel IBIST is a proprietary implementation of a built-in self test (Figure 2). It is being embedded by Intel, Avago and other semiconductor and IP providers into next-generation chips and chip sets. The non-intrusive embedded Intel IBIST functionality can be applied in a number of ways, including structural tests in NBT applications. It can also be used in design-validation applications to confirm the performance of high-speed serial buses on circuit boards. Intel IBIST can test high-speed serial buses such as QPI and PCIe. Test pads cannot be inserted on these high-speed nets because a test pad would disrupt the signal integrity of the board and affect its functional performance. Faults such as micro-cracks, drift in component capabilities across lots or power-supply issues—which might arise because of incorrect or missing capacitors or terminations—can pass low-speed static tests such as ICT or boundary-scan test, but they can cause failures at full functional speeds.

Circuit boards that are based on Intel's newly introduced Xeon Processor 5500 series—which is codenamed Nehalem—provide a useful example of how NBT techniques can be implemented to achieve high test coverage. Figure 3 shows a block diagram of a typical circuit-board based on this processor series. NBT can achieve very high test coverage on this type of board. Test access is provided via the XDP (eXtended Debug Port), a 60-pin, small-form-factor connector that provides access to current and future Intel silicon, system-test resources and debug facilities. Boundary scan, processor-controlled test and Intel IBIST use only a small subset of the available XDP signals. In cases where XDP headers are not available, as in high-volume manufacturing, alternatives can be provided. Boundary scan can provide structural test coverage where it is impossible to insert test pads on the board, such as on the QPI links. Designing boundary-scan into the board can also reduce the number of test points, which will dramatically reduce the cost of fixtures for ICT, flying probe test and other types of intrusive test. In addition, boundary scan can be employed throughout the lifecycle of the system, from design and development, through manufacturing, and including field service and repair.

Processor-controlled test can exercise many of the board's devices and buses with an at-speed functional test, again reducing the need for test points. And because it is a low-level (pre-boot) functional test, processor-controlled test can be run prior to the processor's BIOS or operating system being loaded. As an at-speed test technology, its tests can be applied very quickly when compared to traditional functional tests. Moreover, its diagnostics are excellent. Since Intel has included IBIST's embedded-instrumentation capabilities on this processor series, IBIST tests and tools can also be deployed. For example, the shape and size of a typical eye diagram generated with IBIST margining tests can validate the design's QPI links without placing a probe on these buses. Other validation tests such as bit-error-rate routines can be applied to the design non-intrusively through tools that take advantage of the embedded IBIST.

Meeting the test challenge

Designs based on this processor series are indicative of the challenges facing test technologies. For interconnects and buses such as QPI and PCIe, and high-speed memory links such as those found on DDR3 memories, the older intrusive test technologies are severely limited by the absence of physical test access and by the capacitive signal anomalies that physically probing these links introduces. New non-intrusive board-test technologies leverage the instrumentation that has been embedded within silicon to provide more a extensive test coverage by either complementing the older intrusive technologies or, in some cases, replacing them entirely.

Figure 1: A typical NBT system running a boundary-scan test.
Figure 2: An NBT test station running Intel IBIST eye-diagram margining tests from a laptop.
Figure 3: The block diagram of a typical Xeon Processor 5500 series circuit board.

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