IJTAG standard holds promise for 3D chip test

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For decades since its utterance, Moore’s law has been a given in the chip industry. More of an observation than a dictum, this supposed law states that microprocessors double in performance every 18 months. Now, after holding true for nearly half a century, the years ahead will bring the most serious threat to this trend.

One way of keeping Moore’s law alive will be three-dimensional (3D) multi-die chip packages. Since there really is a physical limit to circuit density in silicon along two dimensions, the next new frontier will be the third dimension. Unfortunately, stacking multiple die in one package increases the complexity of those devices geometrically and threatens manufacturing yield rates.

As a result, effective validation and testing strategies, as well as new industry standards for 3D chips will be essential. Fortunately, formulating a sound 3D chip test strategy is a matter of diligence and foresight. Moreover, several IEEE standards, which have recently been ratified or soon will be, offer hope.

One such specification, IEEE P1687 Internal JTAG (IJTAG), standardizes the interface to validation and test instruments that are embedded in individual die, simplifying their use and deployment, and hastening the development of a marketplace for third-party tools and other related intellectual property (IP).

Strategizing 3D chip test

Fabricating a 3D device involves distinct and clearly identifiable phases. For example, a foundational die must be validated and tested before any other die is stacked on top of it. But the second die in a stack is typically validated and tested on its own before it is added to the stack. This is the known-good-die (KGD) principal.

When two die are stacked, the new stack is often validated and tested again before the next phase in the fabrication process, which may involve adding another die to the stack. Clearly, test re-use and portability from one phase to the next will be essential if costs and yield loss are to remain in check.

Formulating a strategy for validating and testing a multi-die 3D device will require addressing a number of issues involving the three Ws: when, where and what. (The fourth W, why validate and test, is fairly self-evident.)

When are tests performed?

As alluded to, tests will need to be run on individual bare die as well as incomplete and complete stacks of multiple die. Uncovering a fault or failure before another die is attached to a stack can allow for repair work that might otherwise be impossible when the 3D stack is completed and physical access to one of the inner die is impossible.

Correctly timing when an incomplete stack is discarded because it is beyond repair will reduce costs significantly.

For example, if a two-die stack can be discarded before three more die are stacked on top of it, or if wafer-on-wafer stacking can match failing die patterns, the manufacturer is able to recoup significant cost in terms of time and material that might otherwise have been lost.

Where on the device are tests performed?

The upper and inner die in a stack will have no external pins or test pads that might provide access to probes for test purposes. Through-silicon vias (TSV) might be appropriated for test but the test strategy must take into consideration the bandwidth required to apply and run test vectors in a reasonable period of time.

Vectors that require too much time to be delivered from external automatic test equipment (ATE), and then applied and run on the chip will only drive up the cost of the device since the significant portion of test cost is test time. Of course, chip designers will want to minimize on-chip resources dedicated to validation and test; so, one of the first tradeoffs in developing a test strategy for a 3D device will probably involve test time vs. on-chip resources. Another ‘where’ question involves where the TSVs should be placed to facilitate efficient test (and, of course, how many TSVs are needed).

What is the goal of test?

To start with, testing might be intended to validate the design and fabrication of each die so the eventual stack will be composed of known-good-die. Following this phase of die design and manufacturing verification, the goal of test could expand into ensuring that the manufacturing processes related to stacking multiple die, such as back-grinding and laser drilling, have not broken anything in a stack of known-good-die. And then, if TSVs are being used for test, the operation of the test TSVs must be validated before test vectors can be run on them. On top of all this, tests could be conducted to evaluate and investigate new defect and fault models that might only arise in a stacked 3D device, such as vertical connectivity, thermal hot spots, voltage di/dt sensitivity, noise immunity and other potential interactions.

These are just some of the questions that should come up during the development of a validation and test strategy for a 3D chip. Since 3D chip families will differ in stacking techniques, size, on-die content and other factors, the tests that make up test strategies will differ accordingly.

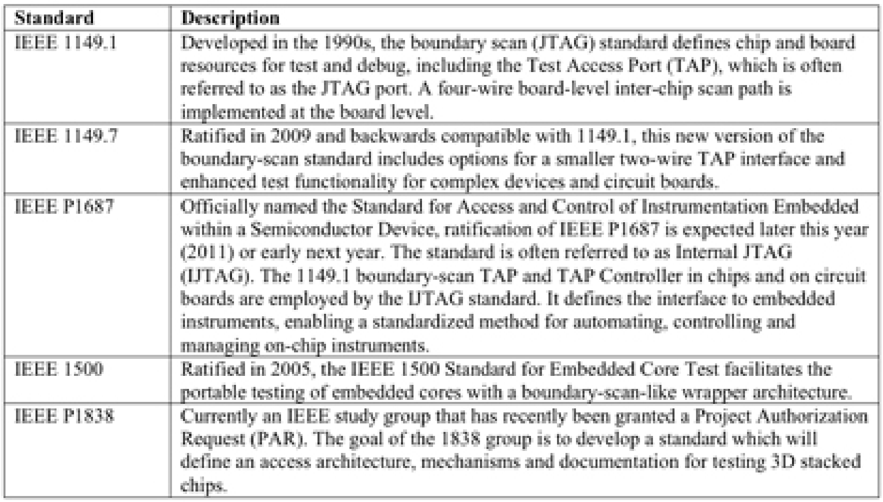
Standardizing validation and test

Several IEEE standards, which are at various stages of development and ratification, will have application to 3D test. One such document in the early stages of development is the new IEEE P1838 Standard for Test Access Architecture for Three-Dimensional Stacked Integrated Circuits.

A working group has been formed with the goal of defining the access mechanism for testing 3D devices. The group is also considering whether it should address new design-for-test (DFT) capabilities involving the management of the new defect and fault models found on 3D chips. The current thinking of the P1838 group is that it will draw on existing and/or soon-to-be-ratified IEEE test standards for its work. For example, the P1838 working group may reference the original IEEE 1149.1 boundary scan (JTAG) standard, the new revisions to the 1149.1 JTAG spec which are in-work now, as well as the IEEE 1149.7 advanced boundary-scan standard that was ratified late in 2009.

The 1149.7 standard reduces the number of signals required for boundary-scan-based communications on a 3D device from the four that were specified in the original 1149.1 specification to just two. These two wires can connect stacked die or embedded IP cores in an 1149.7-based network. Each die and core will have its own network address. Generally, this and other architectural advancements in the 1149.7 standard will allow for more efficient allocation of on-chip resources for validation and test purposes.

Another IEEE specification, the IEEE P1687 Internal JTAG (IJTAG) standard, is expected to be ratified late in 2011 or early next year. This standard will define access mechanisms for embedded on-chip test and debug instruments. It also will become an essential part of 3D validation and test strategies.



Standard	Description
IEEE 1149.1	Developed in the 1990s, the boundary scan (JTAG) standard defines chip and board resources for test and debug, including the Test Access Port (TAP), which is often referred to as the JTAG port. A four-wire board-level inter-chip scan path is implemented at the board level.
IEEE 1149.7	Ratified in 2009 and backwards compatible with 1149.1, this new version of the boundary-scan standard includes options for a smaller two-wire TAP interface and enhanced test functionality for complex devices and circuit boards.
IEEE P1687	Officially named the Standard for Access and Control of Instrumentation Embedded within a Semiconductor Device, ratification of IEEE P1687 is expected later this year (2011) or early next year. The standard is often referred to as Internal JTAG (IJTAG). The 1149.1 boundary-scan TAP and TAP Controller in chips and on circuit boards are employed by the IJTAG standard. It defines the interface to embedded instruments, enabling a standardized method for automating, controlling and managing on-chip instruments.
IEEE 1500	Ratified in 2005, the IEEE 1500 Standard for Embedded Core Test facilitates the portable testing of embedded cores with a boundary-scan-like wrapper architecture.
IEEE P1838	Currently an IEEE study group that has recently been granted a Project Authorization Request (PAR). The goal of the 1838 group is to develop a standard which will define an access architecture, mechanisms and documentation for testing 3D stacked chips.

Table 1: Standards pertaining to 3D chip test

What is IEEE P1687 IJTAG?

Because much of the functionality in a 3D device is quite literally blocked from direct physical contact with the outside world, validation and test strategies must rely on an 'inside-out' approach that employs embedded instruments. Over the last decade or so, chip makers have routinely embedded test and measurement functionality into high-end devices to facilitate their characterization, validation and test.

Now, the performance capabilities of these high-end devices have entered the mainstream or, at the very least, they have become more commonplace in a much larger segment of the computer and communications marketplace. As a result, the industry is realizing that there is a great wealth of test and measurement IP embedded in chips that can be utilized to perform test, debug, monitoring, and other functions more cost-effectively throughout the entire life cycle of systems. The IEEE P1687 IJTAG standard is a step in this direction.

IJTAG streamlines the operations of embedded instruments by defining a standard interface for these instruments and by providing a portable vector description where the vectors are directly associated with the instrument. For design and test engineers, this will simplify the task of using embedded instruments and it will create an opportunity for the development of third-party tools for embedded instruments. In addition, third-parties will likely begin to develop and market their own portable embedded instrumentation IP.

Because the first iteration of the IEEE P1687 IJTAG standard has borrowed from the IEEE 1149.1 boundary-scan standard, P1687 reflects some of the architectural features of boundary scan. The IJTAG standard re-uses boundary scan's TAP and TAP controller. In addition, the IJTAG access network for embedded instruments incorporates a set of registers that is similar to the Test Data Registers (TDR) found in the boundary-scan standard and which comprise a boundary-scan chain see figure 1.

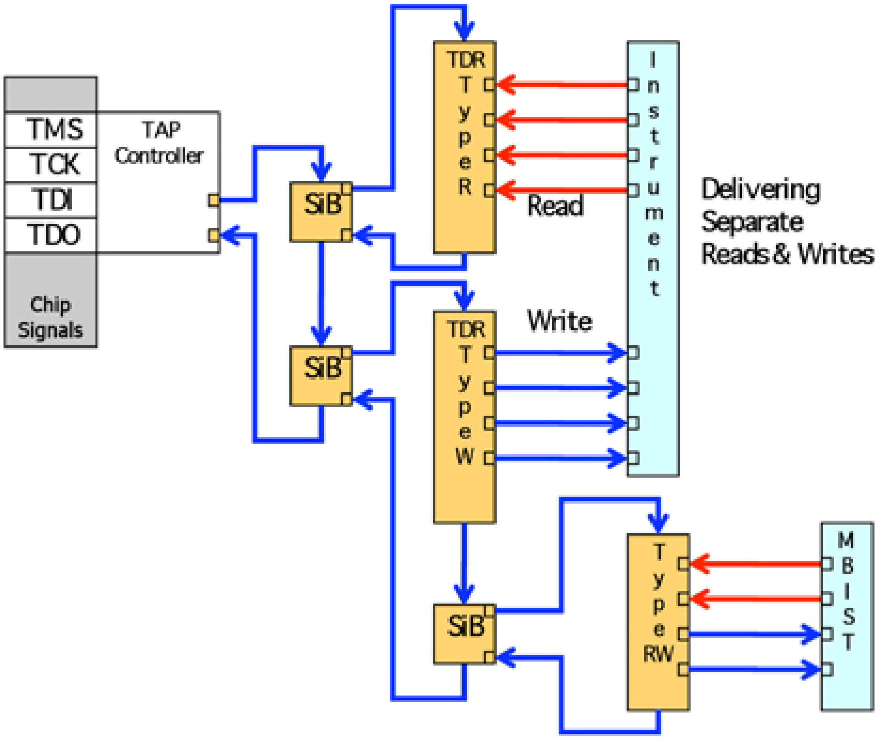


Fig 1: An example of a IEEE P1687 architecture showing IEEE 1149.1 boundary scan TAP controller, its four signals and three instances of P1687's Segment Insertion Bit (SIB).

The IEEE P1687 IJTAG standard is flexible

Boundary-scan and IJTAG scan chains differ from each other insofar as boundary-scan chains are fixed in length and composition while IJTAG networks can be dynamic and variable in their configuration. In fact, segments in an IJTAG scan chain or network can be added or subtracted on the fly. Unlike 1149.1 boundary scan which is based on fixed instructions, the configuration of an IJTAG chain is controlled by the variable data passing through the chain's data registers.

From an architectural standpoint, the IEEE P1687 IJTAG standard is flexible. Consequently, designers can deploy various configurations of an IJTAG network to meet a wide range of engineering tradeoffs involving cost, operational requirements, engineering (area, routing, etc.) and other factors. These architectural configurations are documented by defining them in the IJTAG standard's Instrument Connectivity Language (ICL). ICL essentially describes where the IJTAG TDRs are, the scan paths that access them, how and when these scan paths should vary, the connections between the IJTAG scan path and the boundary-scan TAP controller, and the parallel connections between the embedded IJTAG instruments and the IJTAG TDRs.

One of the real advantages of the IJTAG standard involves test vector re-use. Vectors are written to the instrument interface and can be retargeted to any standardized 1149.1 boundary-scan TAP by processing the ICL to understand the IJTAG access network. This implies cradle-to-grave test vector re-use, beginning with chip-level design verification and continuing through wafer probe, IC package test, circuit board test, system test, yield analysis, and even troubleshooting, debug and repair of end user returns.

The other language that is defined in the IJTAG standard is called Procedural Description Language (PDL). PDL represents the test vectors that are applied directly to instruments and it provides more functionality than standard

1149.1 boundary-scan operations. PDL allows flow-control operatives such as if-then-else, for-next, do-while and others. PDL lets the engineer control and automate the operation and scheduling of embedded instruments, a significant improvement over alternative technologies such as the de facto standard, Serial Vector Format (SVF), which is currently applied at the TAP.

How IEEE P1687 IJTAG can be used to test 3D chips

When it is ratified and adopted by the industry, the IJTAG standard will enable a number of embedded instrumentation functions that will improve the testability of 3D chips.

Of course, the major issue that the IJTAG standard addresses and which the new IEEE P1838 working group is also investigating is how test and debug instrumentation IP will be accessed on a wafer, in an individual die, in partial and completed 3D die stacks, and on circuit boards.

Since boundary scan (IEEE 1149.1) currently provides the physical layer infrastructure for this access, a basic question that remains unanswered at this point is whether each die in a 3D stack will contain a boundary-scan TAP and TAP Controller or whether only one TAP and controller will be deployed in the foundational die. If the latter architecture is deployed, a pure 1149.1 architecture would require a long scan path connecting all the die in a stack.

The one TAP and controller per stack architecture implies that all TAP controller signals (TCK, TDI, TDO, ShiftEn, CaptureEn, UpdateEn, ResetN, and Select) will be distributed to all die in the stack. Further, this would require that the foundational die which has the stack's only TAP/controller can only be designed and fabricated following all other die in the stack since the features of all die must be known to the foundational die so it can support the instructions needed to control the test and debug instruments in the entire stack.

Complicating this further is the fact that a foundational die may be deployed in many different chip configurations. This would mean that some sort of library of instructions might be deployed and in any particular 3D device a certain number of unused instructions might be provided to some die while other die might not have the instructions they needed.

An alternative approach

Another alternative might be to execute an instruction in the 3D stack's one TAP that would select the Test Data In (TDI)-to-Test Data Out (TDO) registers in the daisy chain scan path which connects all of the die in the stack. This is a typical 1149.1 boundary-scan type of architecture. Unfortunately, it would require that practically everything on every die in the stack be active at all times and this would consume a great deal of power. In addition, the length of the scan chain could lead to very long access times, which could increase test times to an unacceptable level. The IEEE P1687 IJTAG standard and its concept of a Segment Insertion Bit (SIB) offers a solution - see figure 2.

While only adding one bit to the scan path, a SIB allows a great deal of flexibility in scan path configuration, including the ability to bypass an entire die. This type of per-die access can be subdivided further on each die with the implementation of additional SIBs for each embedded instrument. This would facilitate the scheduling of embedded instrument operations and enable on-the-fly adjustments to the length of the active scan path.

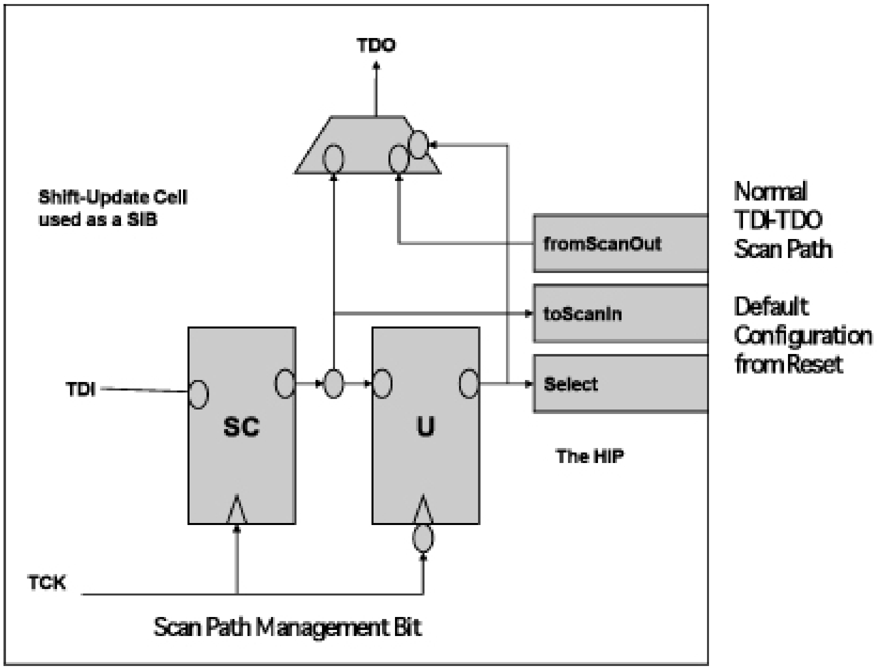


Fig 2: A key element for adding, organizing and managing the operations of embedded instruments is IEEE P1687's Segment Insertion Bit (SIB), which can dynamically alter the length and configuration of a scan path chain.

In a typical 3D die stack with only one TAP and one TAP Controller in the foundational die, SIBs deployed in the upper level die could enable any of the following types of operations- see figure 3:

1. *Bypass* – Exclude this die completely from the 1687 scan chain. This could be no more than a one- or two-bit shift register in the access path.
2. *On-die access allowed* – This action would include the die on which the SIB is located in the 1687 access infrastructure.
3. *Next-die access* – This would include both the die where the SIB is located and include the next die.
4. *Turnaround* – This would terminate the access path at the die where the SIB is located.

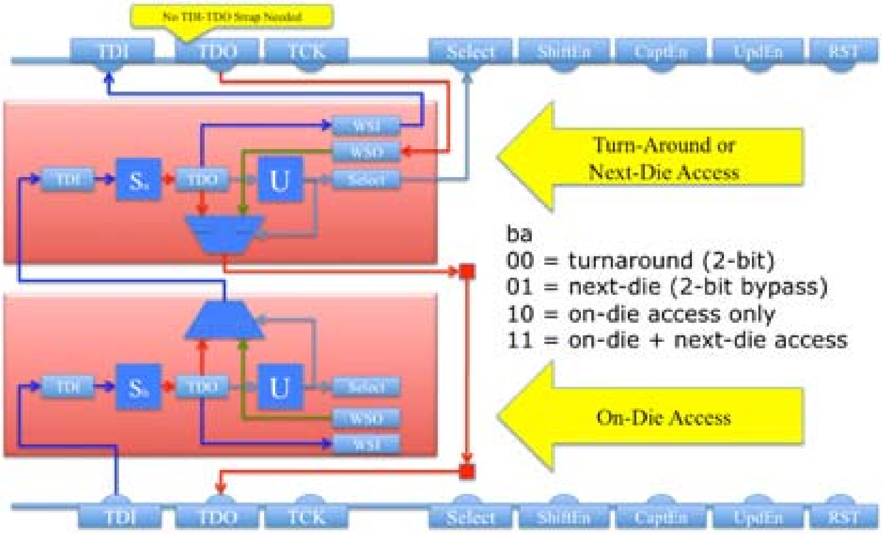


Fig 3: P1687 SIBs can provide functions such as Turn-Around, Bypass, Next-Die and On-Die Access on a 3D multi-die stack with only one TAP and TAP controller on the base die.

Using a TAP/controller on each die in a 3D stack

An alternative to this architecture might involve a TAP/controller on each die in a 3D stack. This makes the die package look more like a circuit board where many chips have their own TAP/controller and are connected in a boundary-scan TDI-to-TDO scan path daisy chain. In such a configuration a die's P1687 network is available on a per-die basis when a die's TAP/controller holds an IJTAG instruction. This would allow each die's TAP to support its own set of instructions.

An example might illustrate how IEEE P1687 simplifies the test and debug process. One test that will be essential for 3D stacked die devices with TSVs connecting each die is some sort of structural electrical test to ensure that the test TSVs are free of opens and shorts. With traditional IEEE 1149.1 boundary scan, this would involve accessing the drive and receive boundary-scan cells on one die while values are applied to the TSV-connected boundary-scan cells on the second die. (A die in the middle of a stack would have an 'up' and a 'down' pair of boundary scan functions.)

Depending upon the architecture deployed in the 3D device, this could be accomplished in either of two manners. First, if each die has its own TAP and controller, several instructions will have to be placed in the TAP/controllers of the two die. Second, if there is only one TAP/controller for all of the die in a 3D device, one instruction will have to select the scan path connecting the two die. With IEEE P1687, this could be accomplished with the placement of one bit in a SIB that adds the needed boundary-scan registers to the active scan chain.

Another base architecture could employ the recently ratified enhanced version of the boundary-scan standard, IEEE 1149.7. Unlike the original boundary-scan standard, IEEE 1149.7 requires an address for each TAP. Data for every TAP are then delivered simultaneously but only those connections with a certain TAP address will react and respond to the transmitted data.

Keeping the options open

These approaches or others could end up being integrated into the standard eventually developed by the IEEE P1838 working group. Since each 3D die stack will have its own set of objectives and tradeoffs, it could be advantageous to have several architectural options for chip designers to choose from. (That is, it may not be possible to formulate a "one size fits all" solution.) This could be feasible since an IEEE P1687 IJTAG operation differs fundamentally from a traditional IEEE 1149.1 boundary-scan operation.

Whereas the target for an 1149.1 boundary-scan operation is a TAP port on a chip, 1500 operations are intended to be applied at the IP core boundary, and P1687 operations are intended for instruments embedded inside a silicon die. This allows silicon suppliers to provide test and/or debug vectors that relate to their own test instruments no matter the access method. P1687 automation tools will use the device's ICL description to bring these vectors either to a die's edge, to the edge of a multi-die 3D device, or to the edge of a board or system that includes the multi-die 3D device.

The immediate task of the 1838 working group will certainly be facilitated by the options available to it. Included among the resources that the working group will be able to draw on will be the years of experience and vast installed base of resources associated with IEEE 1149.1 boundary scan, as well as the influx of new innovation brought about by recently passed or soon-to-be-ratified standards like IEEE 1149.7 and IEEE P1687.

About the author:

In addition to being a chief technologist at ***ASSET InterTech***, Al Crouch is the co-chairman of the **IEEE P1687 IJTAG** working group and an editor for the IEEE P1838 3D test working group. He is a senior member of the IEEE and has filed for more than 30 test-related patents. He currently holds 15 patents.