



ASSET Extends ScanWorks Platform into Chip Test and Verification



November 3, 2009 -- **ASSET InterTech, Inc.** and **SiliconAid Solutions, Inc.** have formed a strategic relationship whereby ASSET will integrate its IC test tool into the ScanWorks platform for embedded instrumentation and resell SiliconAid's insertion and verification tools that support the emerging IEEE P1687 Internal JTAG (IJTAG) standard.

"Beyond this chip debugger that we'll be integrating into the ScanWorks platform, we can see a time when extensive chip tests can be re-used in board and system test, saving manufacturers considerably on test development and shortening time-to-market," said Glenn Woppman, President and CEO of ASSET. "We're also excited about promoting SiliconAid's IEEE P1687 IJTAG tools. We want to encourage the adoption of this emerging standard because we believe it will be critical to the effective utilization of embedded instrumentation in future test and measurement applications."

SiliconAid's JTD chip debugger, which will be integrated into ScanWorks immediately, is a real-time test and debug tool that can monitor structures inside chips and give visibility through an intuitive graphical interface to the engineer who is debugging the device. Although ASSET will initially resell SiliconAid's IEEE P1687 IJTAG synthesis (JTS) and verification (JTV) tools, future plans could call for these tools to be integrated into ScanWorks as well. JTS and JTV let chip designers automatically insert IJTAG capabilities into chips and subsequently verify the implementation. IEEE P1687 provides a standard interface to instrumentation embedded in chips.

"The IJTAG IEEE P1687 standard is not just important for our two companies. It will be critical to the industry as embedded instrumentation proliferates in next-generation device," said Jim Johnson, President of SiliconAid. "Standards like P1687 enable a higher level of integration and automation, beginning with chip design and test, and then transitioning seamlessly into board test. Adding IEEE P1687 IJTAG tools into our suite is a natural next step for us to leverage our existing products and offer more value to our customers."

SiliconAid's SAJE SM Tool Suite

The SiliconAid JTAG Environment (SAJE) is comprised of tools (JTV, JTS, JTD) that focus on chip level JTAG needs for 1149.1, 1149.6, and now IEEE P1687. SAJE SM can be integrated into any major chip design process to handle JTAG requirements. The SAJE SM suite performs semantic checking, simulation-based verification, automatic test program generation (ATPG) and interactive debugging. Now the SAJE SM suite offers these functions in support of the IEEE P1687 standard. SAJESM can leverage design simulation information into automatic test equipment (ATE) and board test with test patterns and an interactive debugger (JTD).

Go to the [ASSET InterTech, Inc. website](#) to find additional information.



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Keywords: ASICs, ASIC design, embedded system design, EDA, EDA tools, electronic design automation, boundary scan, JTAG, microprocessors, MPUs, ASSET InterTech, SiliconAid Solutions,

191/30043 11/5/2009 296 13

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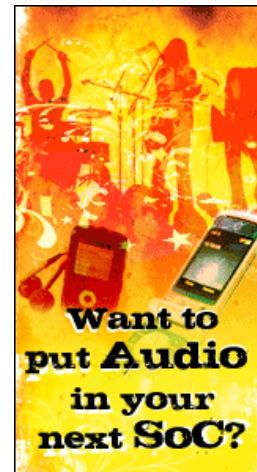


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