

IEEE 1532 CONCURRENT IN-SYSTEM CONFIGURATION

PRODUCT OVERVIEW

The IEEE 1532 Concurrent In-system Configuration product makes in-system configuration of programmable logic devices (PLD) easier and faster. Concurrent PLD configuration not only saves programming time, but it also simplifies the process by incorporating several operations into one. The total programming time for a board or system is often reduced from the sum of the times for programming each device individually to simply the longest time it would take to program any one device. The product is based on the IEEE std 1532™ -2002, Standard for In-System Configuration of Programmable Devices, in which ASSET InterTech played a key role in developing. Support for IEEE 1532 is seamlessly integrated into ScanWorks® so that PLDs from all major vendors can be configured concurrently on the same platform that performs boundary-scan test.

IEEE 1532

The IEEE 1532 standard was developed by a working group of experts from programmable logic vendors, the boundary-scan test industry and suppliers of in-circuit test systems. The mission of the group was “to define, document, and promote the use of a standardized process and methodology for implementing programming capabilities within programmable integrated circuit

devices, utilizing (and compatible with) the IEEE 1149.1 communication protocol. This standard would allow the programming of one or more compliant devices concurrently, while mounted on a board or embedded in a system, known as “in-system configuration.” Concurrent programming may often result in significant programming time efficiencies. The in-system feature would address the need to configure or reconfigure, read back, verify or erase programmable devices after they have been installed by manufacturing process. This eliminates handling damage and the need for manufacturing steps and inventory management related to preprogramming devices.”

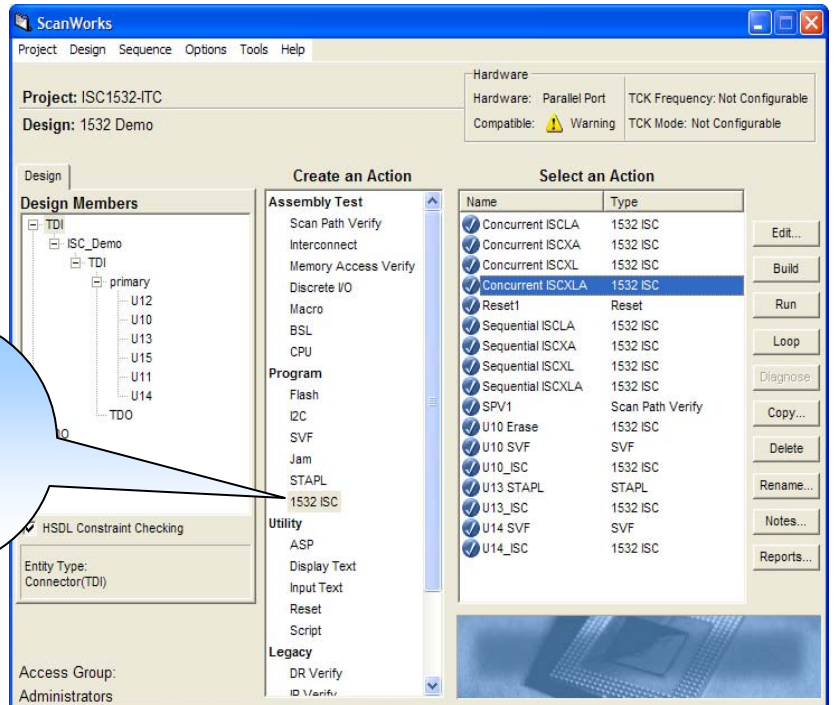
The IEEE 1532 standard was adopted in 2001 and updated in 2002 to include a programming data file format and a method for implementing adaptive programming algorithms. The standard requires that devices comply with the IEEE 1149.1 boundary-scan standard as an infrastructure for describing the algorithms for programming, erasing, verifying, securing and other programming operations for device families. This implies that these devices support the BSDL syntax necessary to describe IEEE 1532 and IEEE 1149.1 features to a boundary scan tools environment like ScanWorks. In addition, the IEEE 1532 standard defines a data format for the data that will be programmed into PLDs. For more detailed

information about how IEEE 1532 is implemented, go to: <http://grouper.ieee.org/groups/1532/p1532.PDF>.

IEEE 1532 CONCURRENT ISC SUPPORT IN SCANWORKS®

Support for IEEE 1532 concurrent ISC is an optional ScanWorks feature that is accessed through distinct ScanWorks actions. IEEE 1532 Concurrent ISC uses the same design description that is used by ScanWorks to perform boundary-scan testing, eliminating any need to re-work design descriptions for IEEE 1532 support. ScanWorks' only requirement for IEEE 1532 support is that the BSDL files used in the ScanWorks design description must include descriptions of the devices' IEEE 1532 features. All PLD

IEEE 1532 Concurrent In-System Programming Action



vendors that support IEEE 1532 provide such BSDL files on their web sites. Moreover, ASSET provides a special web-based library for BSDL files for IEEE 1532 devices.

A ScanWorks IEEE 1532 ISC action has all of the features of every other ScanWorks action. It can be defined and applied on a ScanWorks development station or included in a test sequence that will be applied by a ScanWorks manufacturing station. An IEEE 1532 ISC action can also be called from a custom user interface developed with ScanWorksAPI or the Process

Automation Scripting API. From the IEEE 1532 ISC action dialog, the user selects the devices to be programmed and the IEEE 1532 programming data files for each device. Then the programming operations to be executed for each device and any necessary preconditions are set. Lastly, if more than one scan path is present on the design, the scan path that will be activated for the ISC action is designated.

Define a 1532 ISC Action

Action Name: Concurrent ISCXLA

Precondition:

Target Scan Path(s): primary

Reset before running precondition:

Reset after running action:

Use concurrent programming:

Target Device(s): Active (selected), Bypass

Device	Action	Data	Read Back	Read Back CRC
U13	PROGRAM	decount_v2.isc		
U14	program	A-G.ISC		
U10	program	decount_2.isc		

Specify Device Configuration

Device: U13

Data: decount_v2.isc

Read Back:

Read Back CRC:

Actions: PROGRAM

- TEST_VERIFY_IDCODE
- PROC_ENABLE
- PROC_ERASE
- TEST_BLANKCHECK
- PROC_PROGRAM(array)
- TEST_VERIFY_PROGRAM(array)
- PROC_PROGRAM_DONE
- PROC_DISABLE

IMPLEMENTING IEEE 1532 CONCURRENT ISC OPERATIONS

ASSET has implemented support for In-System Configuration using IEEE 1532 by partnering with Xilinx and Lattice. In its ispVM[®] System software, Lattice Semiconductor has implemented support for concurrent

in-system configuration for all IEEE 1532-compliant devices except for those that require “Adaptive” algorithms. Xilinx has provided support

for devices that use adaptive algorithms in their J-Drive™ tools. In order to ensure that our customer have the best tools for their applications ASSET has incorporated the Lattice ispVM software and the Xilinx J-Drive software into ScanWorks. By partnering with Xilinx and Lattice, ASSET is able to deliver a fully tested, low risk solution for the concurrent programming of IEEE 1532 devices.



The ispVM System software is used when the 1532 ISC action is selected and J-Drive tools are used when the 1532-Adaptive action is selected. If the BSDL file for a IEEE 1532 compliant device includes the LOOP command, then the 1532-Adaptive action must be used. If it does not include the LOOP command, then either the 1532 – Adaptive or the 1532 ISC action can be used. Both actions are included in the IEEE 1532 Concurrent ISC product and both are enabled when the 1532 ISC product license is available.



SUPPORTED DEVICE FAMILIES

Note: The Xilinx System ACE is not programmable. Early Virtex/ and Spartan-II/III are not supported. Support is not yet implemented for the most recent Spartan-3A or Spartan-3A DSP families. Support is still being refined for the Platform Flash PROMs.

- Xilinx**
- CoolRunner-II CPLDs
 - XC9500 CPLDs
 - XC9500XL CPLDs
 - XC9500XV CPLDs
 - XC18V00 PROMs
 - Spartan-3 FPGAs
 - Spartan-3E FPGAs
 - Virtex-II FPGAs
 - Virtex-II Pro FPGAs
 - Virtex-4 FPGAs
 - Virtex-5 FPGAs

Altera

- EPC Family
- MAX 3000 Family (EPM3)
- MAX 7000 Family (EPM7)

Lattice

- ispMACH 4000B
- ispMACH 4000C
- ispMACH 500-VG
- ispLSI 2000VE
- ispLSI 2000VL
- ispMACH 4A3
- ispLSI 5000VE
- ispGDXVA

Highlights

- Significant reduction in board/system in-system configuration times
- Simplify programming operations
- Combine PLD in-system configuration with boundary-scan test operations
- Uses industry proven ispVM from Lattice Semiconductor