ASSET INTERTECH

Guidelines for Chip Design For Test (DFT) Based on Boundary Scan or JTAG

Prepared by

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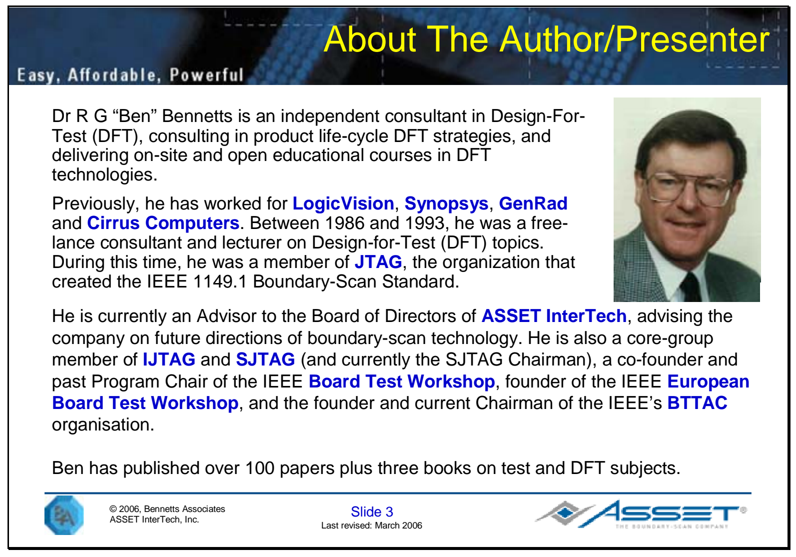
for ASSET InterTech, Inc.

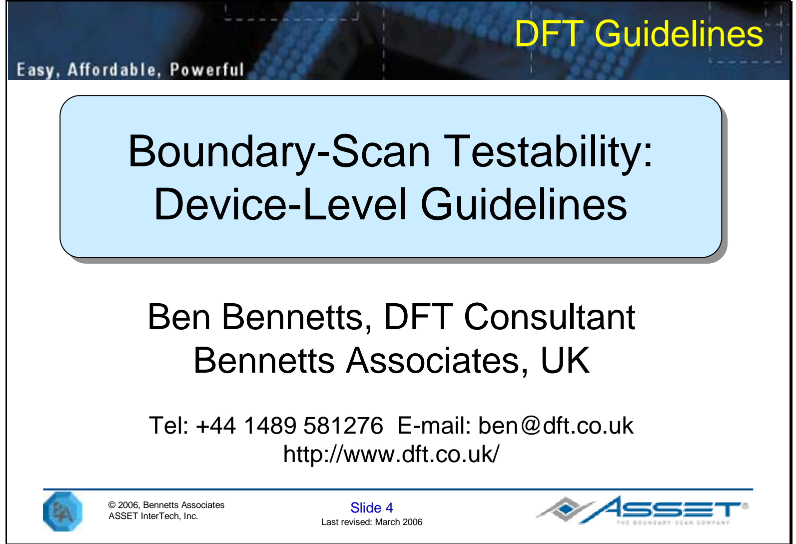
April 2006

ABSTRACT:

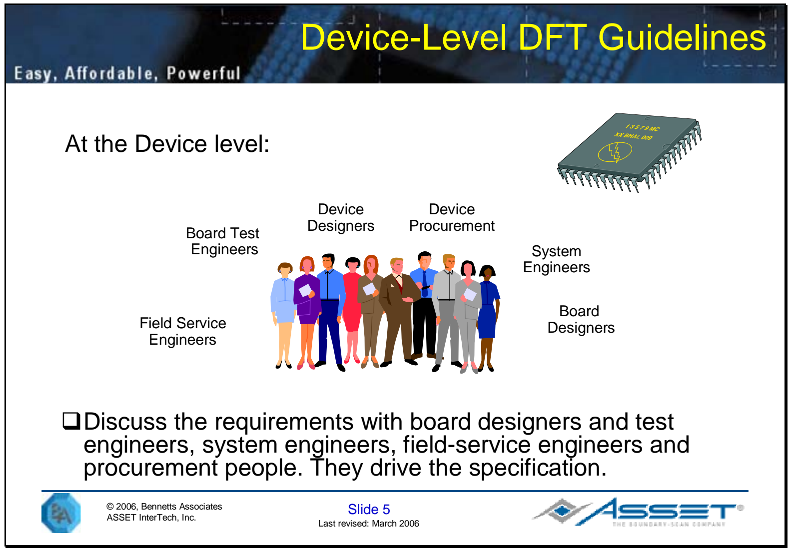
This document is DFT Guidelines for devices to be tested primarily through the use of boundary scan/JTAG, based on the IEEE 1149.1-2001 Standard.

Any comments, corrections, suggested additions should be sent to the author, Ben Bennetts, at **ben@dft.co.uk**.



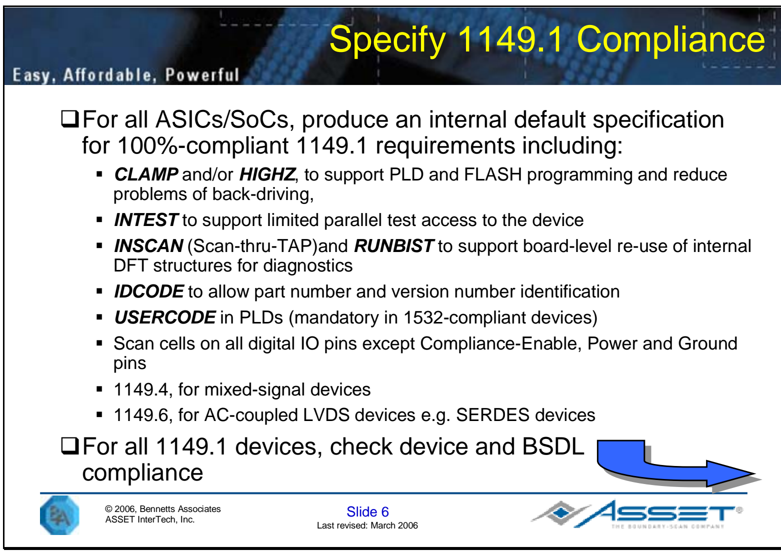


In this document, we will look at DFT guidelines specific to the design of devices to be tested through the boundary-scan (JTAG) registers of IEEE 1149.1-compliant devices. Since the 1149.1 structures are incorporated inside the compliant devices, many of the guidelines relate to the specification of optional features inside the devices i.e. are device-level DFT guidelines. Accordingly, the first part of the document considers the device-level guidelines.



First and foremost, we should ask "who drives the specification for JTAG/boundary-scan features inside new ASICs and SoC devices?". The answer is "all those who will benefit from the use of boundary scan" – that is, prototype board debug engineers, board test programmers, system integrators, and field service repair engineers. It's also worth adding device procurement people to the group. This makes such people conscious of the need to buy 1149.1-compliant devices. Consequently, the correct way to specify the 1149.1 features in a new ASIC or SoC is for all these people to sit down and decide the product life-time strategy for testing the boards. Each engineer will have a different view of the requirements specification and, collectively, the group can try to come up with a consensus view of the overall requirement, but note: obtaining a consensus view can be difficult!!

Once specified, the requirement can be presented to the chip designer in the form of a BSDL file. But note that some 1149.1 chip-level boundary-scan (JTAG) synthesis programs cannot accept BSDL as an input specification. Check with your vendor.



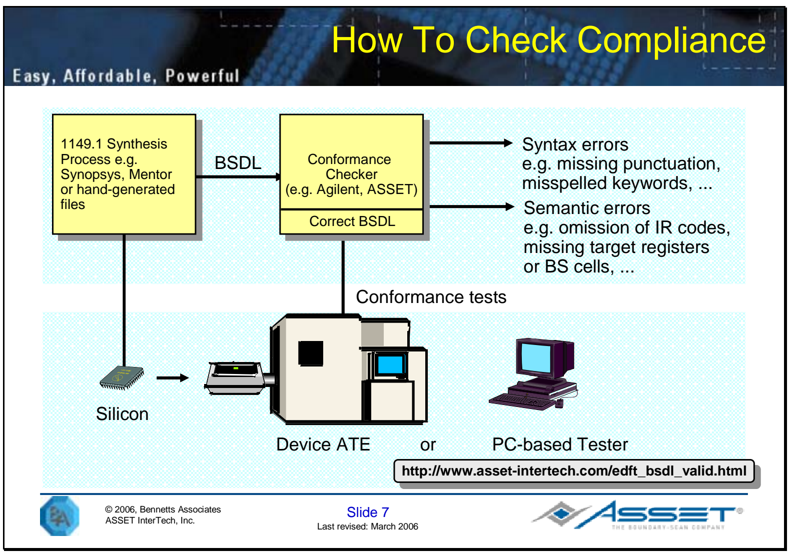
All devices should be 100% compliant with the 1149.1 Standard.

It is a good habit to specify all the optional public instructions (e.g. IDCODE, CLAMP, HIGHZ, etc) by default and only remove them if it can be shown that they will never be used or that they cause violation of another design requirement. IDCODE allows identification of the device manufacturer plus the part number and version number. It also supports a higher-quality board-level scan-chain integrity test.

IC vendors should have checked all 1149.1 features before shipping the parts to system companies. Make sure they have done this. You do not want to find a faulty 1149.1 part once it has been bonded to the board.

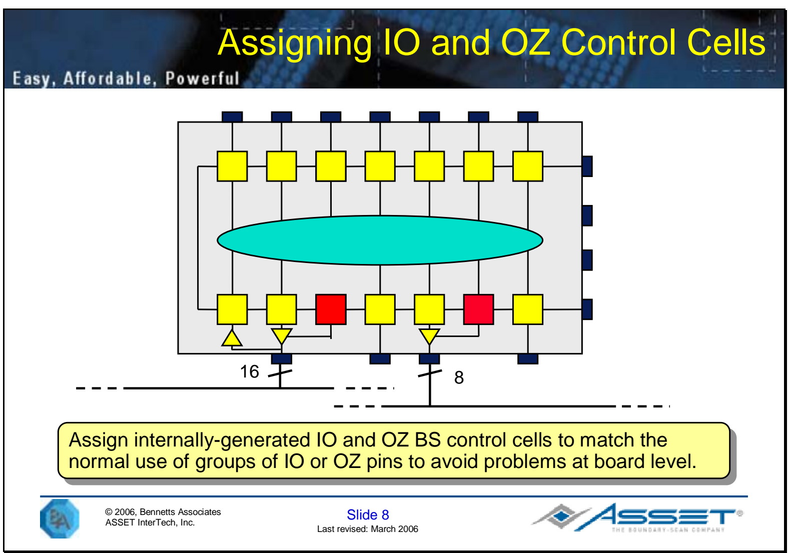
Strictly speaking, there should not be any non-compliant 1149.1 devices!! But, if the vendor has done something that does not comply (tying TRST* low inside the device is a common non-compliant feature), make sure the non-compliance is documented. Non-compliance can be documented in the Design Warnings section of a BSDL file.

Last, but not least, validate the BSDL files – next slide.

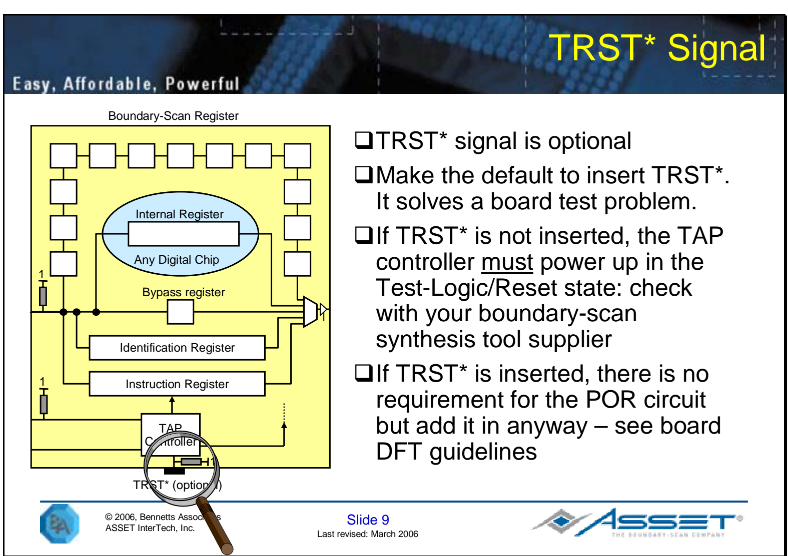


As you will appreciate, the BSDL files must be 100% accurate. Any slight error in the data can completely disrupt the board-level pattern generation processes and cause anomalous behavior which can become very difficult to diagnose correctly. It is strongly recommended that BSDL files are checked both syntactically and semantically before they are used by the board-level pattern-generation and pattern-application processes. There are commercial checkers available, from companies such as ASSET InterTech (www.asset-intertech.com).

The final proof of correctness is to compute 1149.1 conformance tests from the apparently correct BSDL, and then apply these tests to a device on either a chip tester or even a PC-based tester. You are strongly urged to carry out both the syntax and semantic tests, and then to generate and apply conformance tests on real silicon before using BSDL files “in anger”.

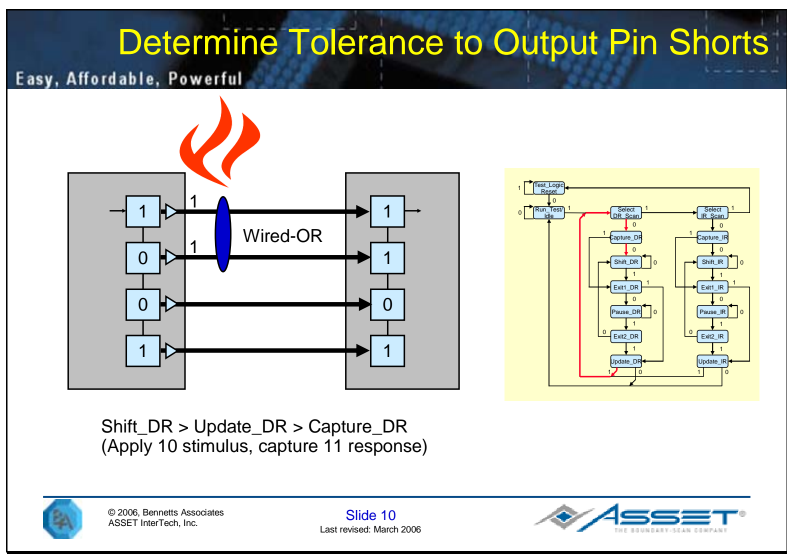


Bidirectional (IO) and three-state (OZ) pins require status-control JTAG or boundary-scan cells so that their status can be controlled whilst the device is in its test mode. Often the status control is based on an input pin, such as an *Output_Enable* pin. If the control is internal, extra boundary-scan (JTAG) cells are inserted in the JTAG register. Such scan cells should control the IO and OZ pins is a way that conforms to the natural use of the IO or OZ pins. This prevents unnatural test configurations at board level that might place other on-board devices into a potentially dangerous state.



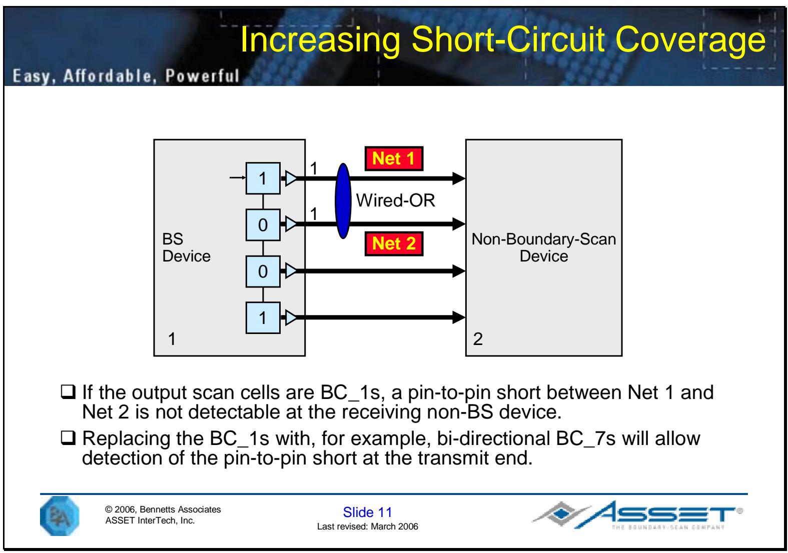
TRST* is an optional active-low asynchronous reset signal for the 1149.1 logic. There always exists a synchronous reset, initiated by holding the TMS signal at logic 1 and applying five consecutive TCK clocks (the so-called “TMS = 1, 5 x TCK” cycle) but, as we will see later when we reach the board guidelines section, there

are very good reasons to also incorporate the optional TRST* feature. There are also very good reasons to insert a Power-On-Reset (POR) circuit to the TAP controller even if the optional TRST* is inserted. Note: POR is not mandated if the TRST* signal is inserted.

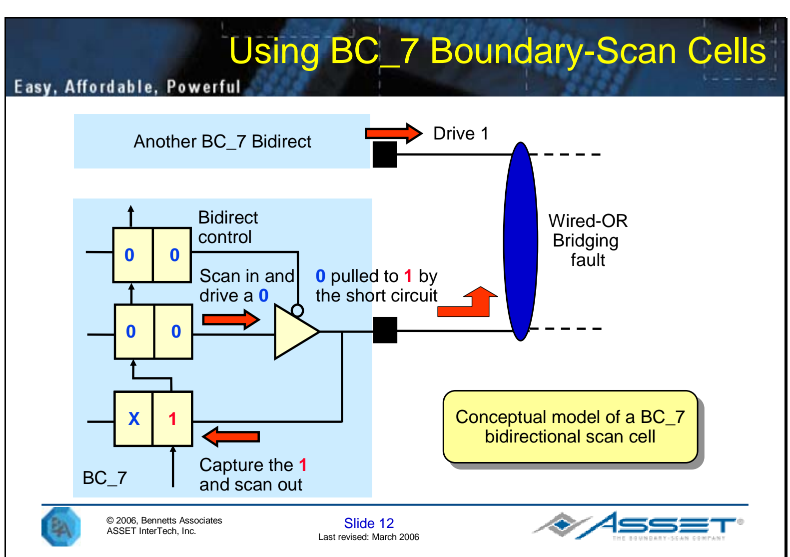


It is ironical that the only way to find pin-to-pin shorts at the board level is by deliberately creating contention on two driver scan cells i.e. causing one driver to drive a logic 1 and the other to drive a logic 0. If the short is present, then we assume that it is either a strong-1 weak-0 (Wired-OR) short or weak-1 strong-0 (Wired-AND) short. Such a test places a stress on the output drivers since one output will dominate, forcing the other to its opposite logic value and possibly damaging the output drive amplifier of the weaker signal. In the world of in-circuit test, this problem is known as *node forcing* or *back driving* and steps can be taken to reduce the amount of time the outputs are under stress. In the JTAG or boundary scan world, the time it takes to apply all the interconnect tests is a function of the complete length of the boundary-scan/JTAG chain, the number of interconnect patterns, and the frequency of TCK. This time may become too long and irreversible damage can occur to one of the output drivers. You will need to determine the vulnerability of the outputs to such damage.

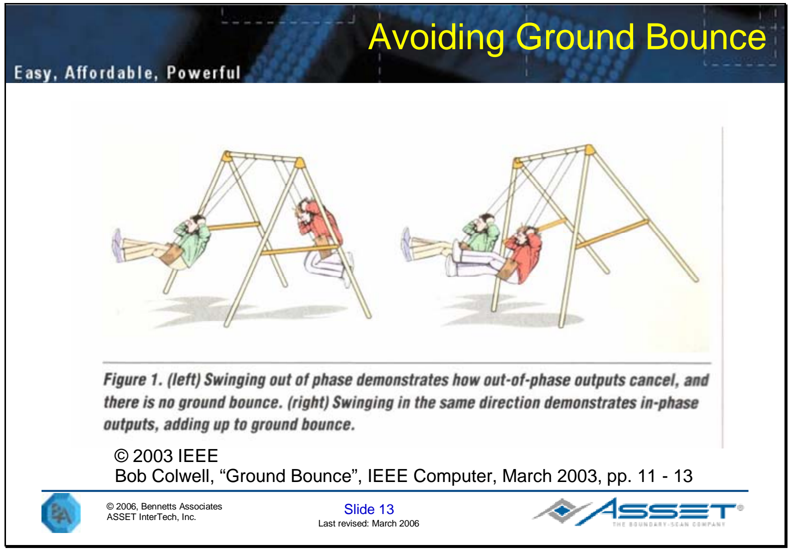
In the example above, the assumption is that the short behaves like a strong 1 weak 0 (Wired-OR) short, and the initial 10 stimulus values in the driver scan cells are received as 11 response values in the sensor scan cells. Once the received values are off-loaded from the board, the presence of the short will be known.



The figure shows a JTAG/boundary-scan device connected to a non-boundary-scan device. The existence of the short is not detectable by the boundary-scan/JTAG structure if the output boundary-scan cells are drive-only cells e.g. BC_1s. The pattern can be set up and applied but there is no JTAG/boundary-scan visibility of the response values. Consequently, there will be a loss of defect coverage unless the driver scan cell can also become a sensor. This can be achieved by replacing the drive-only boundary-scan cells with drive-and-sense boundary-scan cells, such as a BC_7: next slide



The BC_7 scan cell is especially designed for bidirectional signal pins and when in Drive mode, it is able to Sense the value of the driven signal i.e. the BC_7 is a self-sensing boundary-scan cell. Using BC_7s instead of BC_1s will allow detection of shorts between boundary-scan (JTAG) and non-boundary-scan devices, thereby increasing the defect coverage on the board.



An interesting way of illustrating the phenomenon of ground bounce.

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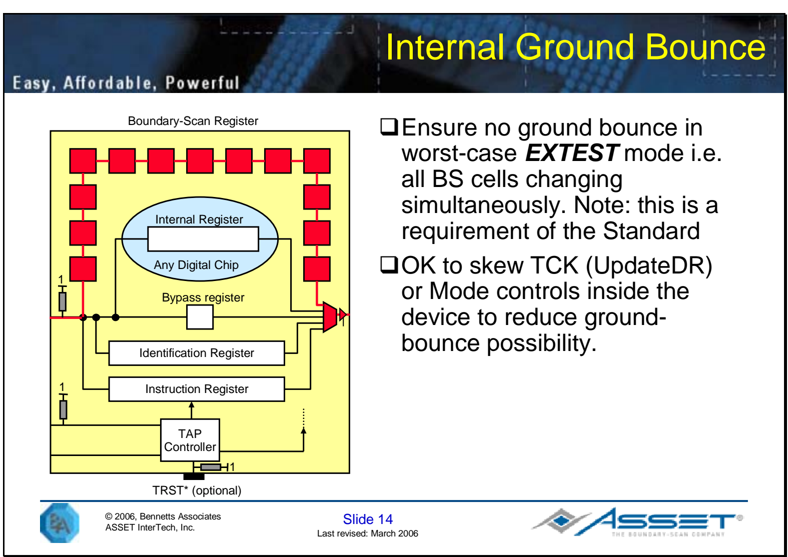
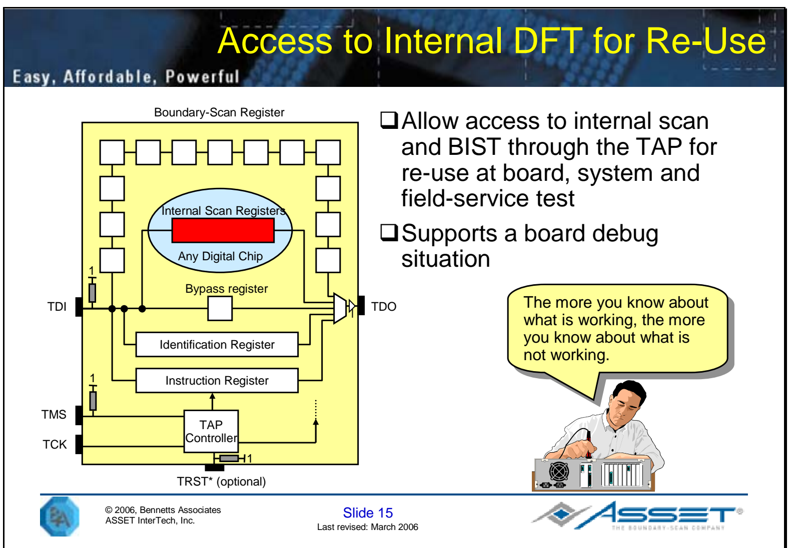
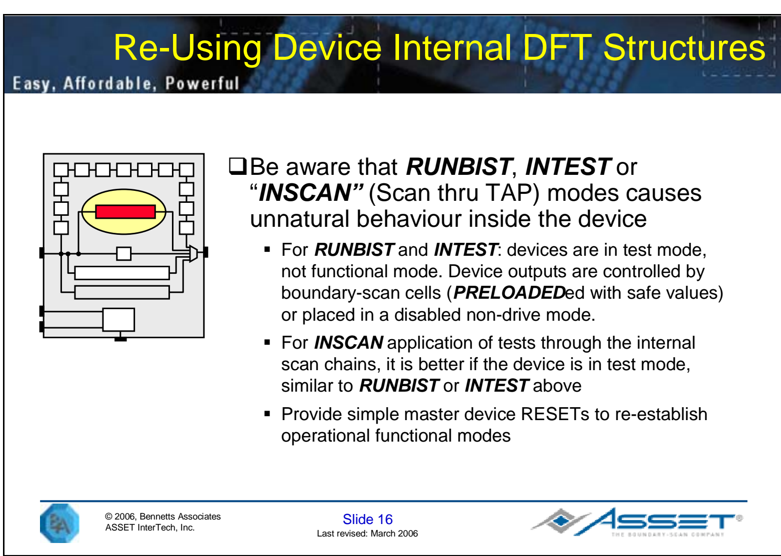


Ground bounce is a dip in the DC supply voltage caused by a sudden power surge and, if it occurs it can disrupt the operation of the TAP controller. The 1149.1 Standard states that there should be no ground bounce inside a compliant device under worst-case switching conditions in the JTAG (boundary-scan) cells – for example, if all output scan cells were updated from, say, all-1s to all-0s. It's interesting to ask whether an 1149.1 synthesis tool actually checks this requirement!!

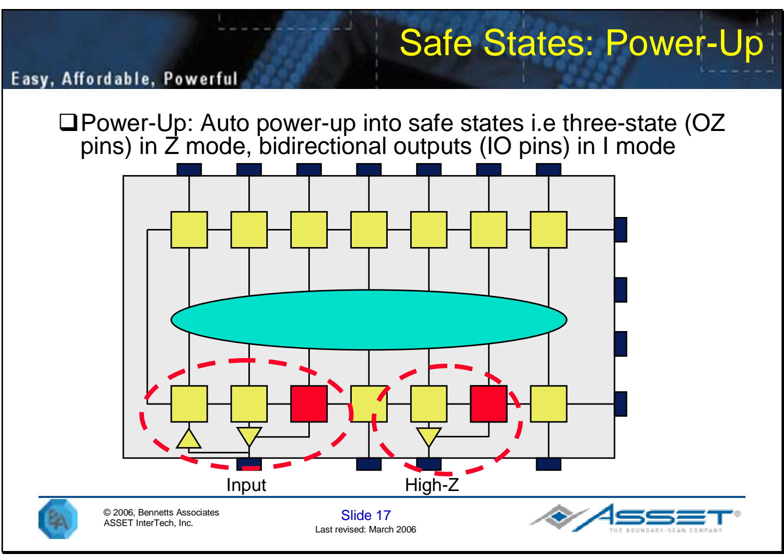


Allowing access to other internal chip DFT features, such as internal scan (known as *Scan Thru TAP*) and internal memory BIST or logic BIST (using RUNBIST-like instructions) allows re-use of these features once the chip is assembled to the board. Such re-use supports improved board-level diagnostics.

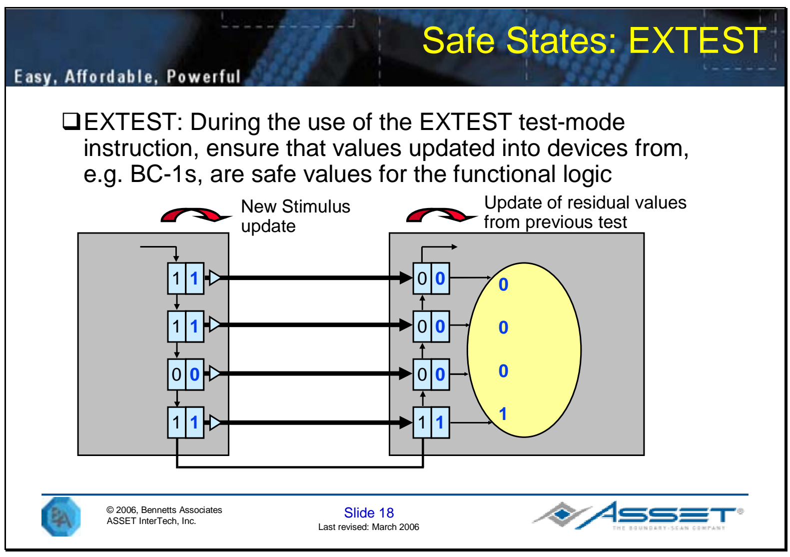


Using the optional RUNBIST or INTEST public instructions places the device in test mode. The outputs of the device are under the control of the boundary scan/JTAG register cells and can either be preloaded with safe values (using the PRELOAD instruction) or placed in a disabled non-drive (high impedance) state.

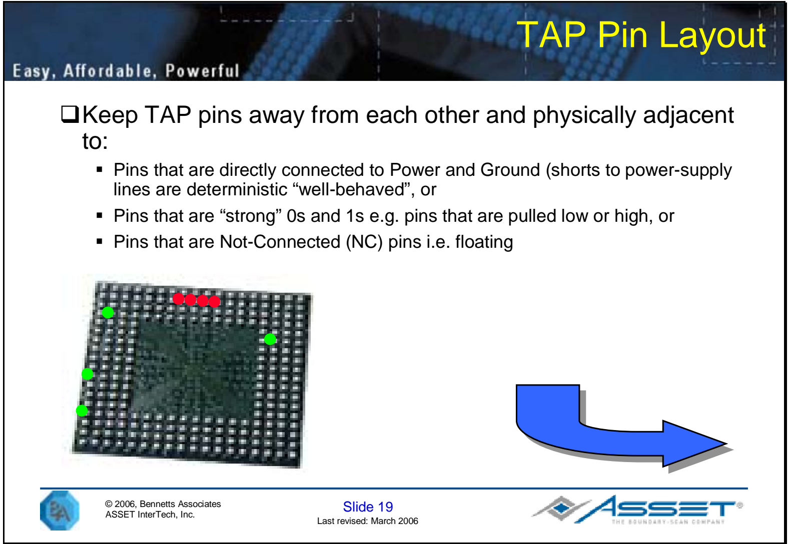
Using private instructions such as “INSCAN” to access internal scan paths (sometimes called “Scan Thru TAP”), the values driven out of the device output pins should also be under the control of the JTAG/boundary scan register cells and can either be preloaded with safe values (using the PRELOAD instruction) or placed in a disabled non-drive (high impedance) state.



In general, it is desirable that boundary-scan (and non-boundary-scan) devices power up in safe states. That is, three-state outputs power up with their outputs in the high-Z state, and bidirectional outputs power up in the input mode rather than their output drive mode. In this way, the risk of powering up into a state of contention (bus fight) is reduced. Safe-state power up can be achieved by internal power-on circuitry (preferred) or by controlling *Output_Enable* control cells via their boundary-scan/JTAG cells and using the PRELOAD instruction during board initialisation (not so good as the board may power up in an unsafe state to start with).

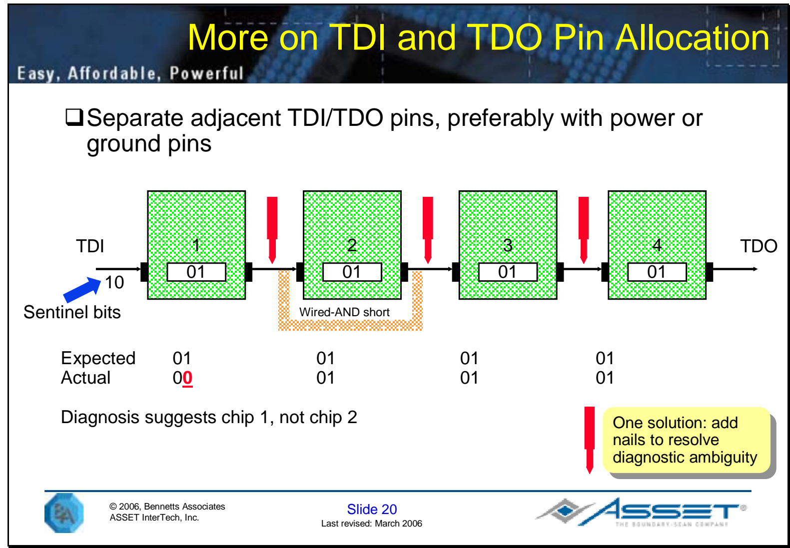


During the update operation of test-mode instructions, such as EXTEST, values on BC_1 or BC_2 input scan cells are updated into the functional logic. Ensure that the board-level interconnect pattern-generation algorithm will generate safe values into the functional logic (difficult) or, alternatively, ensure that the functional logic can accept any input from the boundary-scan (JTAG) cells without the risk of damage (easier).



Placing TDI, TDO, TMS, TRST* and TCK pins close to Power and Ground pins means that shorts will behave very deterministically as strong stuck-at-1 or stuck-at-0 faults appropriately. It also reduces the risk of crosstalk thereby creating higher signal integrity, especially on TCK.

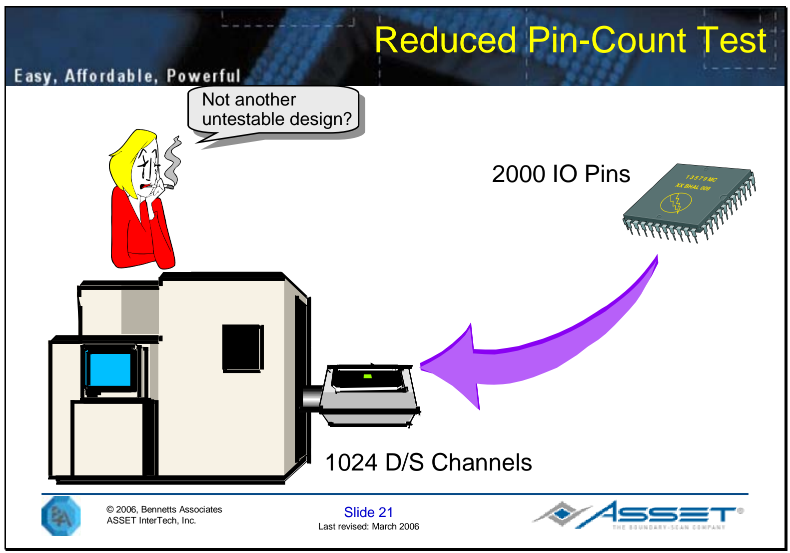
The next slide illustrates how a short between an adjacent TDI and TDO pin, although detectable, can create an incorrect diagnosis.



In this example, the TDI and TDO pins of Chip 2 are assumed to be shorted together during the integrity test based on placing the Instruction Register in the active path and capturing and shifting out the captured hardwired 01. If each instruction register is just 2 bits long (the minimum length) and the short behaves like a Wired-AND short, then the actual values will differ from the expected values but the diagnosis suggests that the problem is associated with Chip 1, not Chip 2.

Note: if the short behaves like a Wired-OR short, the detection will occur on the second sentinel bit. The reader is invited to "check out the 1s and 0s". The reader is also invited to see what would happen if the alternative integrity test, based on selecting the default Identification or Bypass register, is applied.

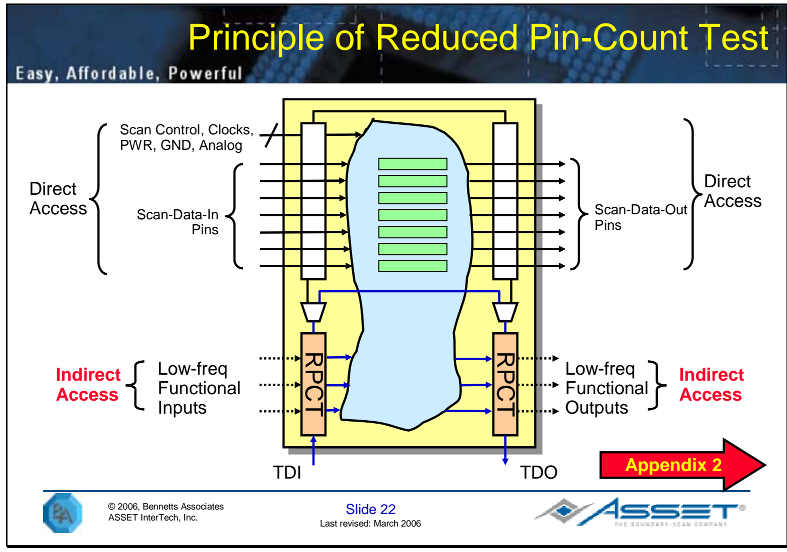
Note: if there is an open between a TDO-to-TDI connect, this will result in all downstream values becoming logic-1s because of the requirement for an open-circuit TDI to rise to logic 1. Detection of the open is not difficult but diagnosing the source of the open is ambiguous – is it at the exit TDO pin or the entry TDI pin? Diagnosis to the source of the open-circuit is assisted if the TDO-to-TDI interconnect can be probed, either with a bed-of-nails probe (in-circuit test or flying probe) or more simply with an oscilloscope probe. Adding a test point to the TDO-to-TDI interconnect facilitates the use of a 'scope probe.



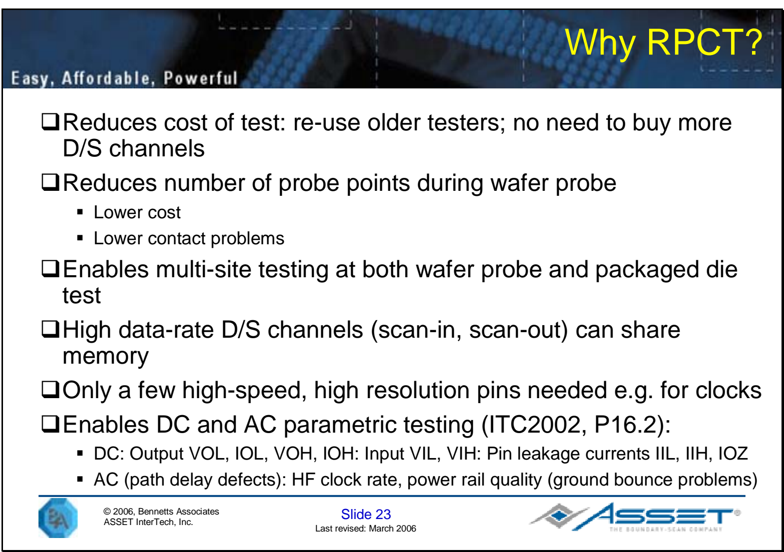
Problem:

How to test a 2000-pin chip on a 1024-Driver/Sensor channel tester?

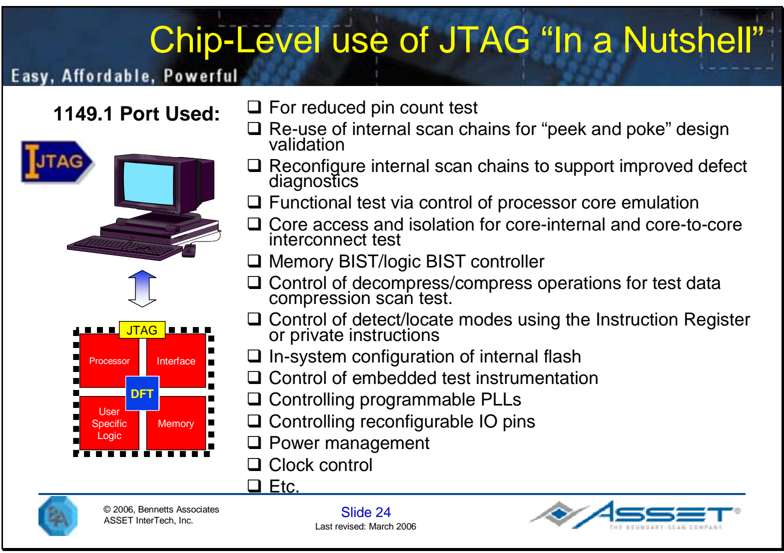
Solution 1: Buy another 876 DS channels at $2K each (= $1.752M extra capital investment)
Solution 2: Use 876 bits of the JTAG (boundary-scan) register to indirectly access the low-frequency pins, at zero extra cost. Called Reduced Pin Count Test (RPCT)



Reduced pin count test (RPCT) is becoming popular as a way of keeping down the cost of test for devices that are “fully loaded” with internal scan, BIST and 1149.1 boundary scan or JTAG. Companies such as IBM, Motorola and now Philips are using part of the boundary-scan/JTAG register to access the low data-rate functional pins of a device in lieu of engaging these pins through a dedicated driver/sensor pin channel. High data-rate pins, such as Scan-In, *Scan-Out* and *Clock* pins are contacted directly. The boundary-scan or JTAG register is designed to allow segments to be addressed through the TAP using private instructions, such as INTEST-RPCT. The addressed segment is used for serial-to-parallel access on the input side, and parallel-to-serial access on the output side. The remainder of the boundary-scan register is left in transparent mode.



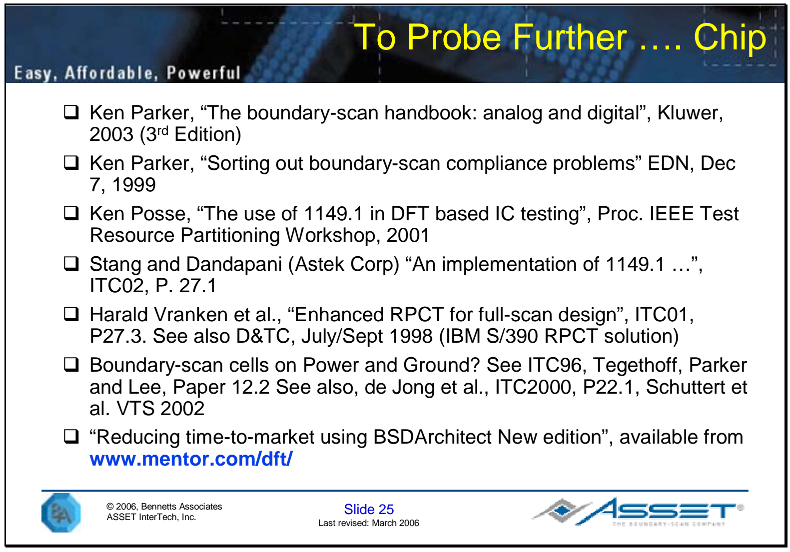
The slide summarises some of the advantages of RPCT.

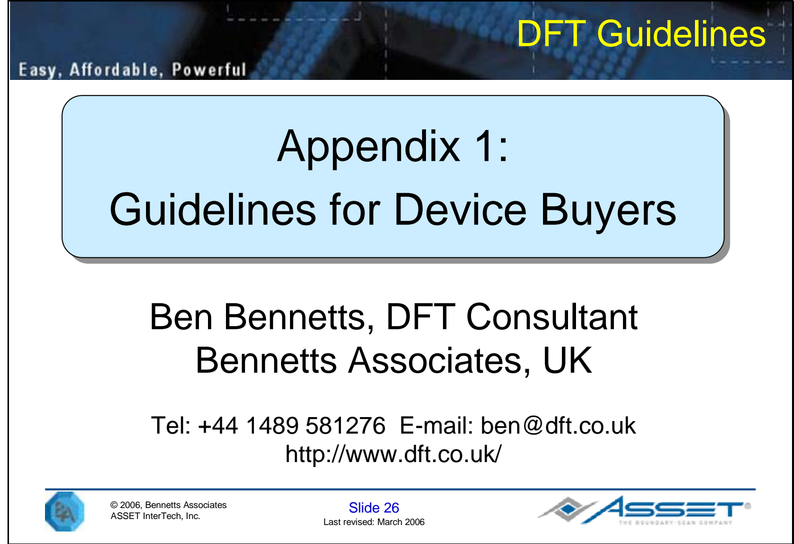


Chip designers are using the IEEE Std 1149.1 (JTAG) Test Access Port not just for its intended purpose of providing access to boundary scan test functions, but increasingly as a way of gaining access to a variety of internal test features for prototype chip design validation and structural test purposes. This trend is of great interest across the industry, from IP providers to EDA and ATE companies to system integrators. Providing for and gaining access to on-chip test features helps address a wide range of test challenges. While IEEE Std 1149.1 provides very generic support for internal test access, these new applications have begun to stretch the architectural requirements of IEEE Std 1149.1 and have clearly pointed out the need for better methods of describing and accessing internal test features. In response, an *ad hoc* group has decided to take a closer look at what chip designers are implementing, what problems they are encountering with TAP-based access, and what extensions would be useful to them. Once the problems are understood, it may be possible to develop standard solutions.

Jeff Rearick (Agilent Technologies) kicked off the IJTAG initiative at ITC 2004. The objectives of the group are to understand the full range of "new" device-level applications of IEEE Std 1149.1 i.e. the "what" and "why", and then to understand the current limitations of 1149.1 that either prevent or make it difficult to use 1149.1 in a specific way. Currently, it is <u>not</u> the intention of the group to determine whether the 1149.1 Standard should be upgraded one more time. Essentially, the objectives of the group are to standardize the protocols and associated tools without compromising compliance to the 2001 version of the Standard.
The unofficial name for the initiative is IJTAG, where "I" stands for Internal i.e. the use of JTAG for device-internal applications. (You may also hear the initiative referred to as I-JTAG, iJTAG, 1149.i or 1149.x. IJTAG is preferred.) At the moment, the activity is focused on the needs of the designers and the test engineers of prototype High End-ASICs and SoCs.

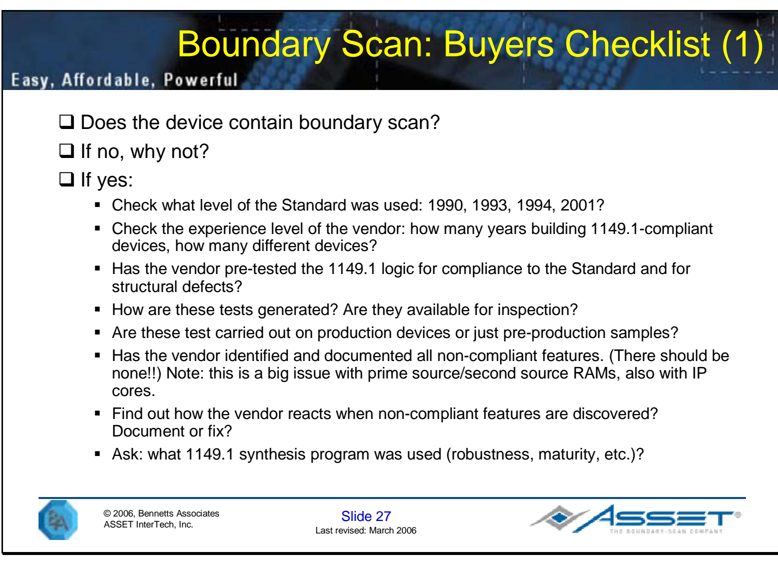
The next public IJTAG meeting will take place at the 2005 VLSI Test Symposium, http://www.tttc-vts.org/ If you are planning to attend VTS, this will be an opportunity for you to find out more. In the meantime, please register your interest in IJTAG by sending e-mail to Jeff Rearick at jeff_rearick@agilent.com.

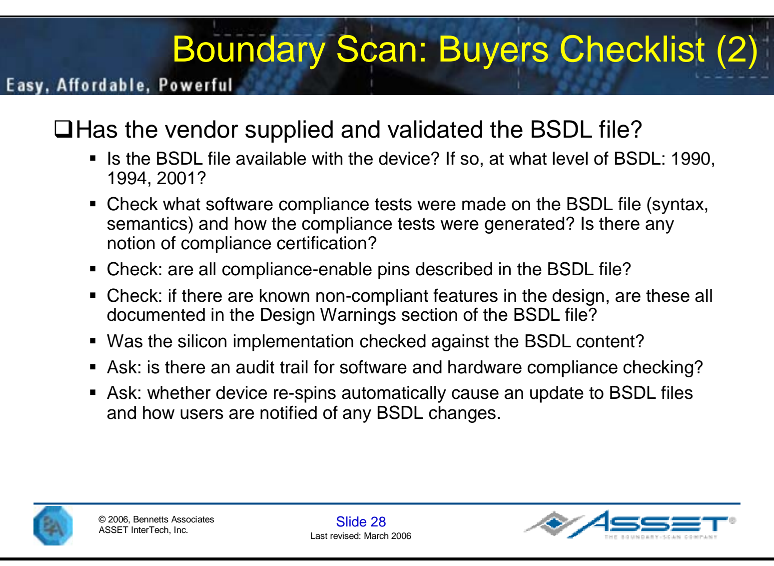


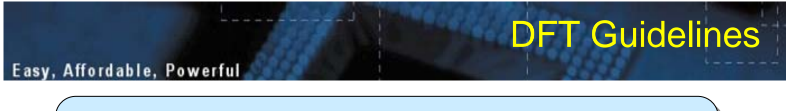


This appendix contains a summary of guidelines for people who are not deep into the technicalities of boundary scan/JTAG but whom; nevertheless, influence the purchase decision to buy boundary-scan devices e.g. corporate buyers.

This Buyer's Checklist is designed to sensitise Buyers as to the importance of making sure that they purchase devices containing JTAG/boundary scan.







Appendix 2:
Reduced Pin Count Test

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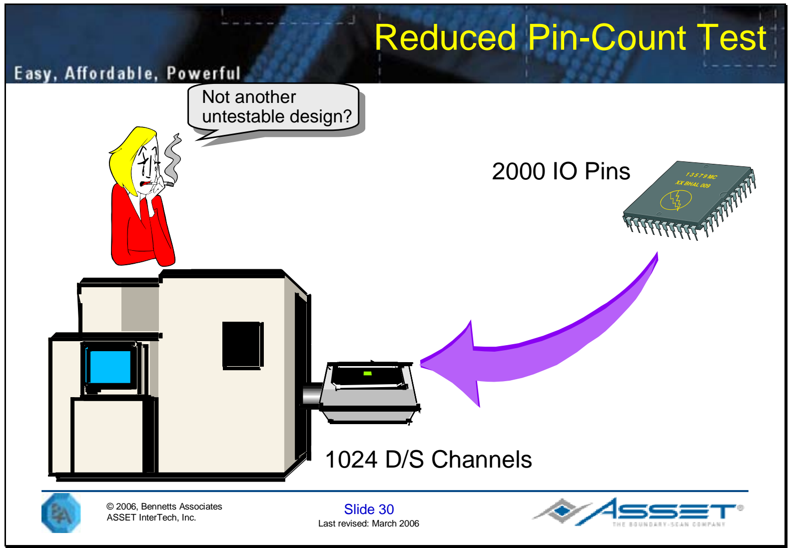
This appendix contains more information on Reduced Pin Count Test.



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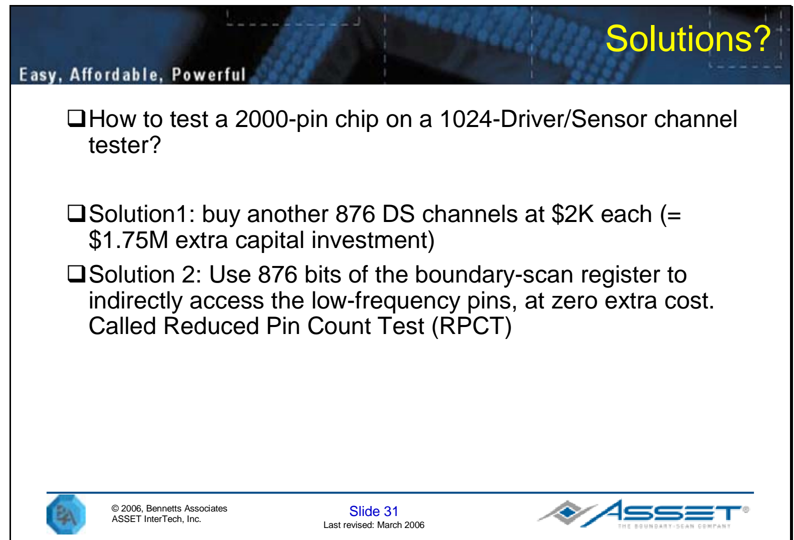

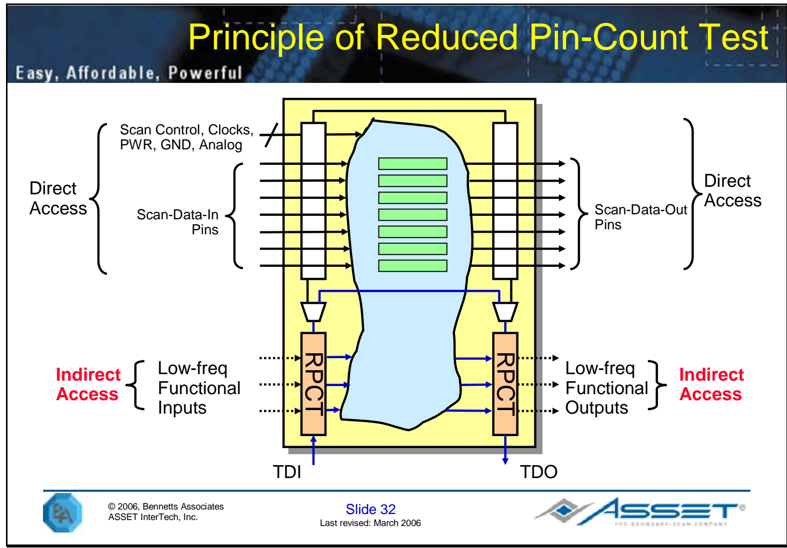

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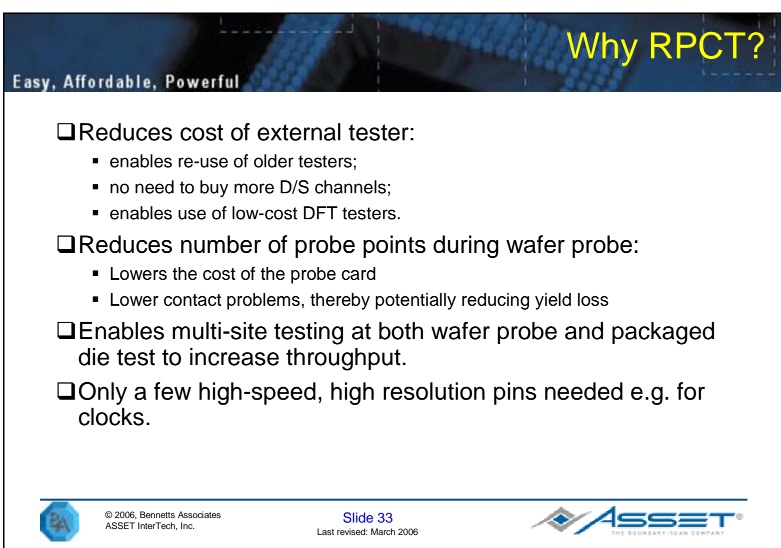
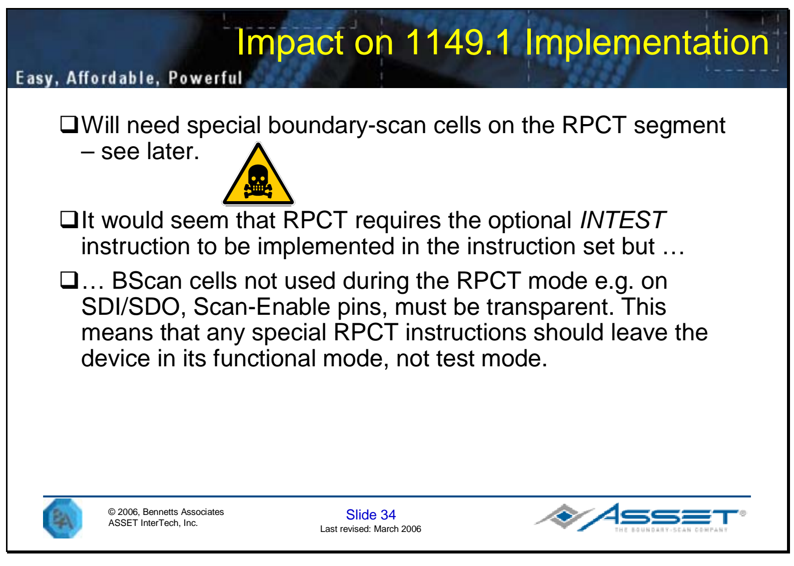


The slide summarises some of the advantages of RPCT.


Impact on 1149.1 Implementation
Easy, Affordable, Powerful
❑Will need special boundary-scan cells on the RPCT segment – see later.
❑It would seem that RPCT requires the optional INTEST instruction to be implemented in the instruction set but …
❑… BScan cells not used during the RPCT mode e.g. on SDI/SDO, Scan-Enable pins, must be transparent. This means that any special RPCT instructions should leave the device in its functional mode, not test mode.
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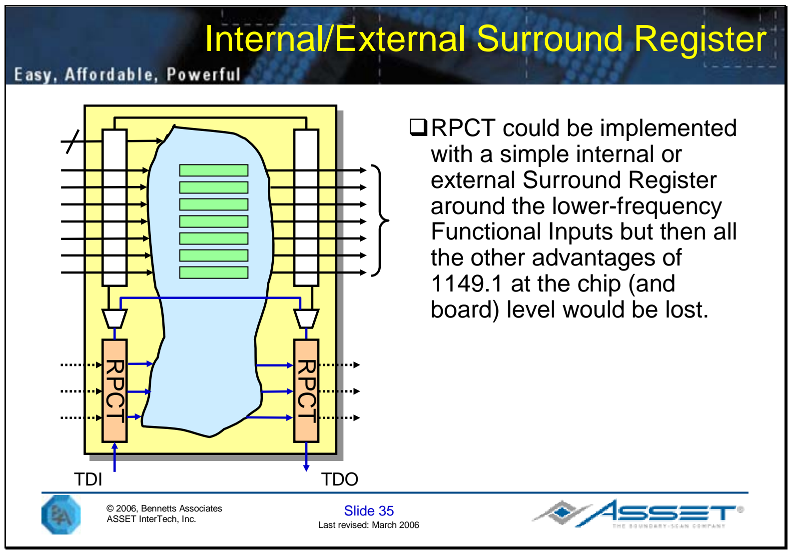
Internal/External Surround Register
Easy, Affordable, Powerful
RPCT
RPCT
TDI
TDO
❑RPCT could be implemented with a simple internal or external Surround Register around the lower-frequency Functional Inputs but then all the other advantages of 1149.1 at the chip (and board) level would be lost.
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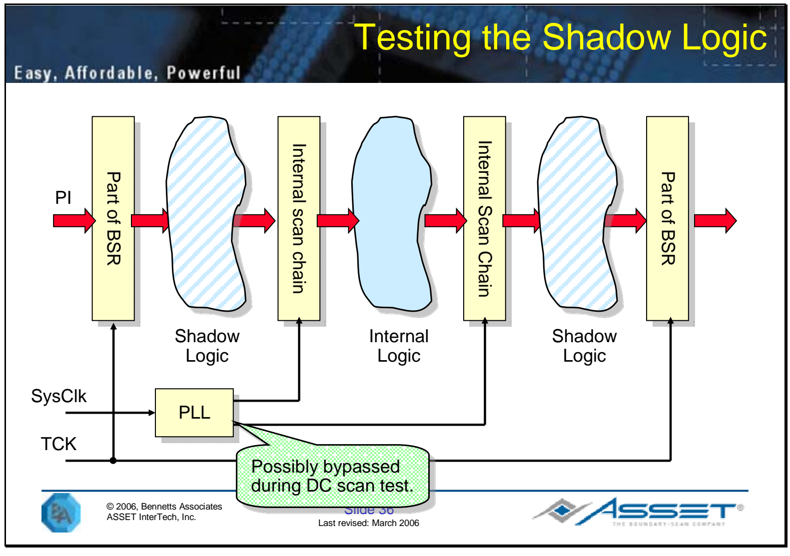
Testing the Shadow Logic
Easy, Affordable, Powerful
PI
Part of BSR
Internal scan chain
Internal Scan Chain
Part of BSR
Shadow Logic
Internal Logic
Shadow Logic
SysClk
PLL
TCK
Possibly bypassed during DC scan test.
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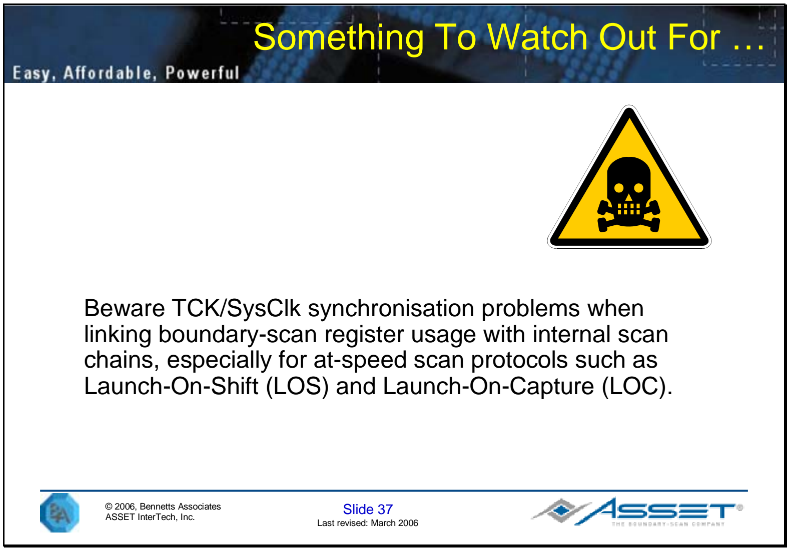
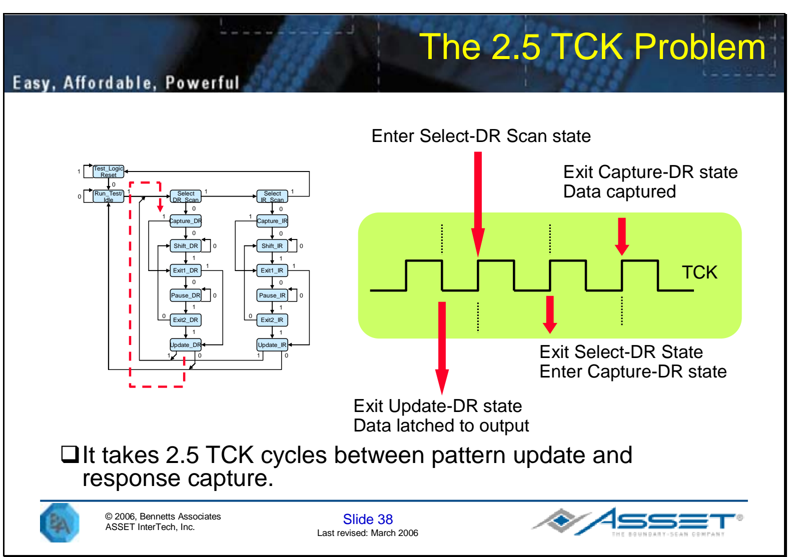
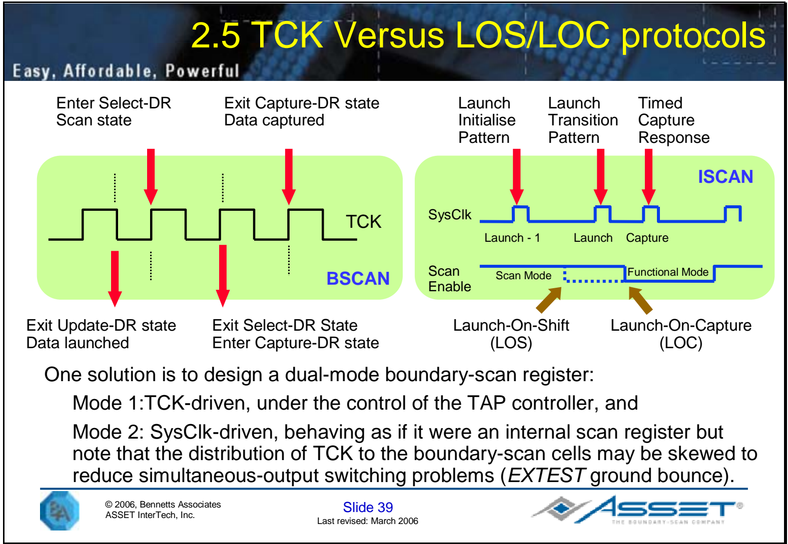


BSCAN and ISCAN work with different clocks and different protocols. These differences can cause major problems of synchronisation in an RPCT environment.

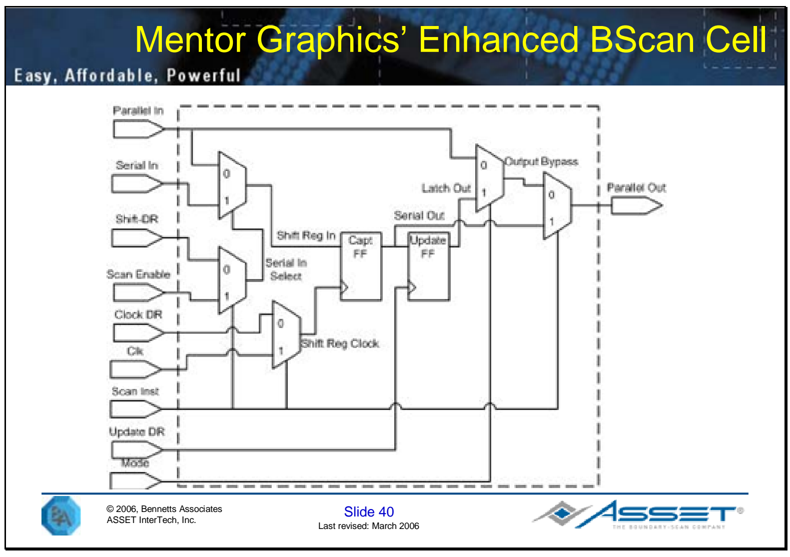


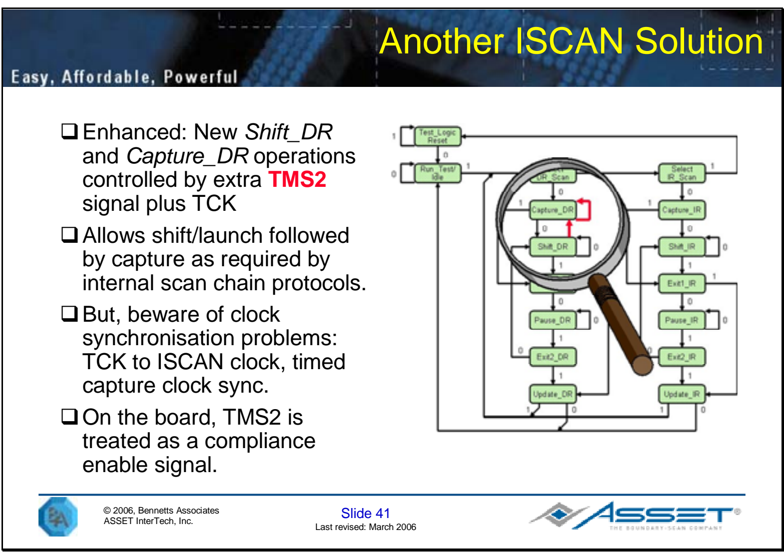
The time between the exit of the Update-DR state (launch of the pattern) and the enter Capture-DR state (capture of the result) is 2.5 TCKs. This limits the ability to do at-speed testing across interconnects.

At the time of writing, there is only one proprietary solution on the marketplace – LogicVision's At-Speed Interconnect (ASI)



The problem is to synchronise the use of the segment of the boundary-scan (JTAG) register with the internal scan-chain protocol. One solution is to design the boundary-scan register to have dual modes: one based on the 1149.1 TAP controller protocol and under the TCK clock, and another where the register is under the control of the internal scan-chain clock (SysClk) and is fully synchronised with the internal scan chains.

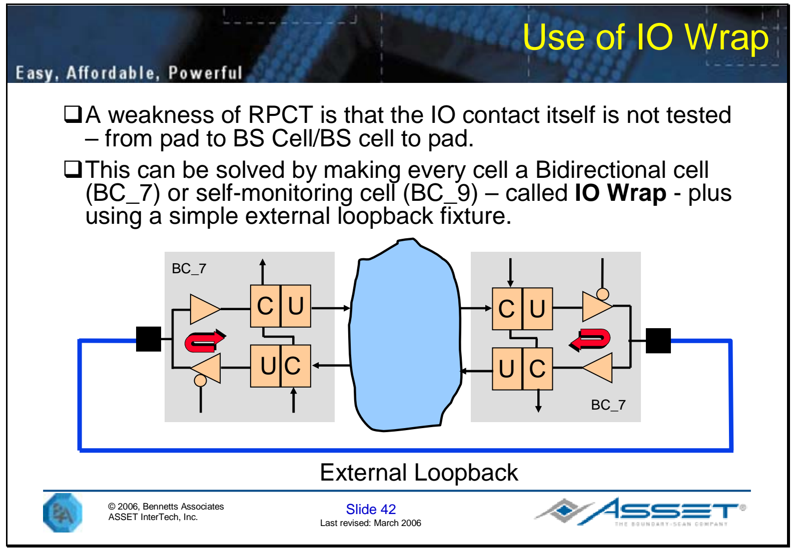




The diagram shows the 16-state state table for the TAP controller. The value on the state transition arcs is the value of TMS. A state transition occurs on the positive edge of TCK and the controller output values change on the negative edge of TCK.

The TAP controller initializes in the ***Test_Logic Reset*** state (***"Asleep"*** state). While TMS remains a 1 (the default value), the state remains unchanged. In the ***Test_Logic Reset*** state and the active (selected) register is determined by the contents of the Hold section of the Instruction register. The selected register is either the Identification register, if present, else the Bypass register. Pulling TMS low causes a transition to the ***Run_Test/Idle*** state (***"Awake, and do nothing"*** state). Normally, we want to move to the ***Select IR_Scan*** state ready to load and execute a new instruction.

An additional **11** sequence on TMS will achieve this. From here, we can move through the various ***Capture_IR***, ***Shift_IR***, and ***Update_IR*** states as required. The last operation is the ***Update_IR*** operation and, at this point, the instruction loaded into the shift section of the Instruction register is transferred to the Hold section of the Instruction register to become the new current instruction. This causes the Instruction register to be de-selected as the register connected between TDI and TDO and the Data register identified by the new current instruction to be selected as the new target Data register between TDI and TDO. For example, if the instruction is ***Bypass***, the Bypass register becomes the selected data register. From now on, we can manipulate the target data register with the generic ***Capture_DR***, ***Shift_DR***, and ***Update_DR*** control signals.


Use of IO Wrap
Easy, Affordable, Powerful
❑A weakness of RPCT is that the IO contact itself is not tested – from pad to BS Cell/BS cell to pad.
❑This can be solved by making every cell a Bidirectional cell (BC_7) or self-monitoring cell (BC_9) – called IO Wrap - plus using a simple external loopback fixture.
BC_7
C U
U C
C U
U C
BC_7
External Loopback
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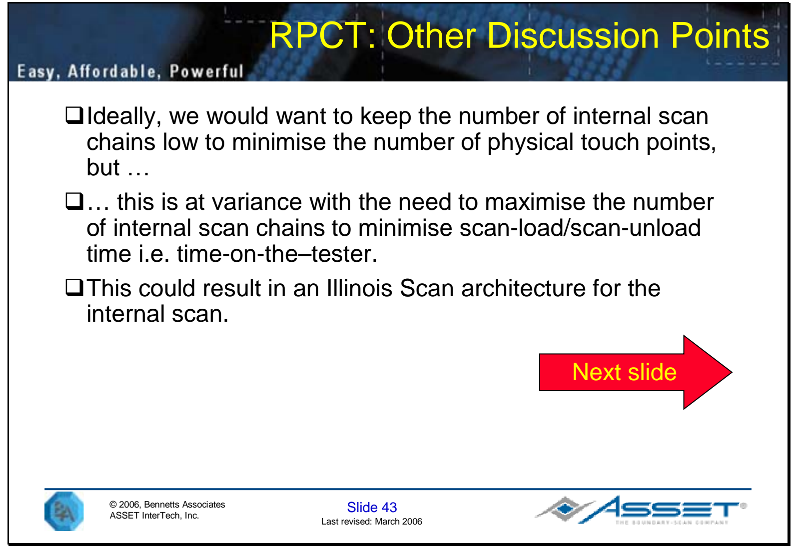
RPCT: Other Discussion Points
Easy, Affordable, Powerful
❑Ideally, we would want to keep the number of internal scan chains low to minimise the number of physical touch points, but …
❑… this is at variance with the need to maximise the number of internal scan chains to minimise scan-load/scan-unload time i.e. time-on-the–tester.
❑This could result in an Illinois Scan architecture for the internal scan.
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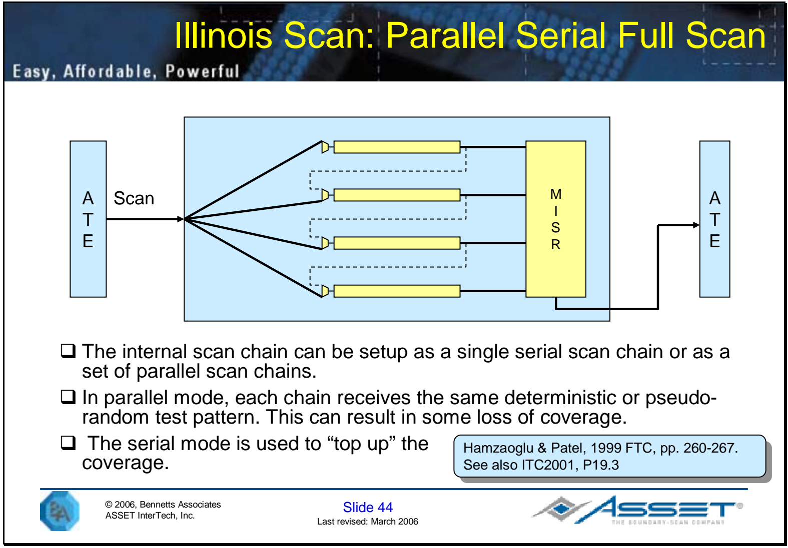


Features of VirtualScan

Patent-pending virtual scan technology for broadcasting external scan chains to user selectable number of shorter internal scan chains and compacting them back into original number of external scan chains.

Automatically inserts broadcaster and compactor circuitry

Outputs complete virtual scan netlist

Includes tools for scan insertion and synthesis

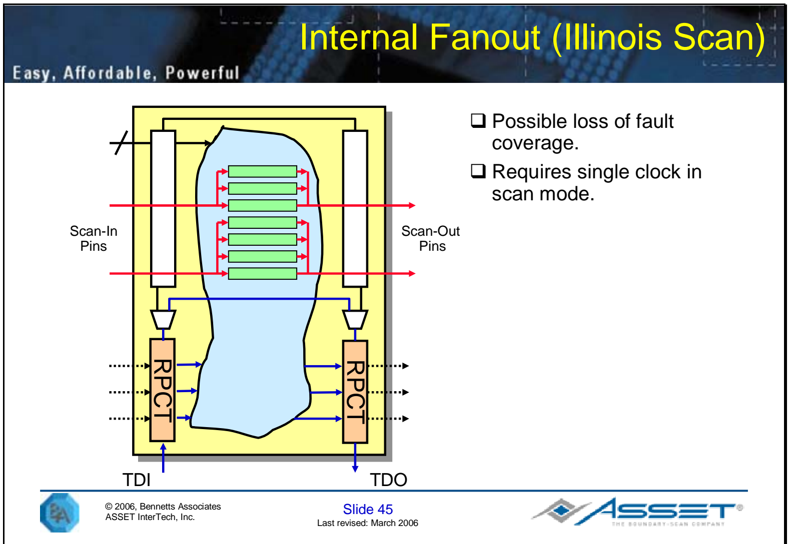
Uses an enhanced virtual scan ATPG

Static and dynamic compaction of ATPG patterns

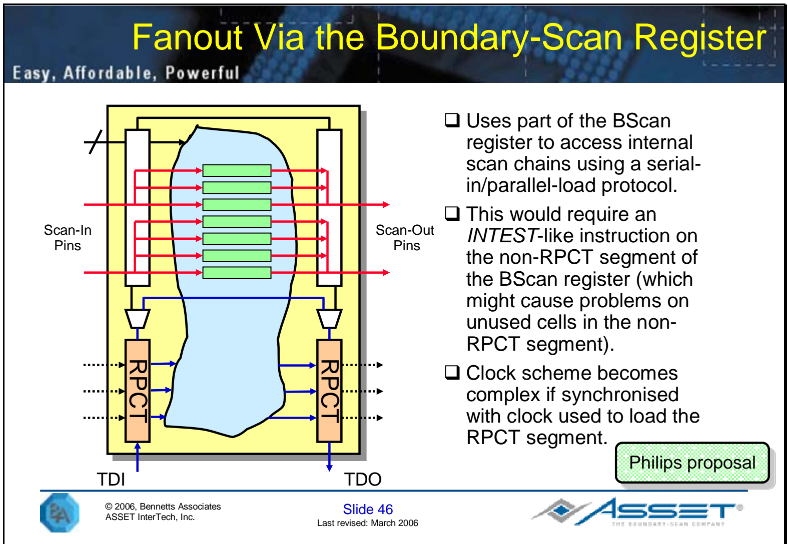
Advanced multiple clock domain handling using proprietary multiple-capture-per-cycle scheme

Can be used with scan chains inserted using third party tools

Fully compatible with SynTest's existing DFT tools as well as TurboDebug-SOC/Scan and TurboDiagnosis-Scan for debug, diagnosis and failure analysis of scan chains.



Reduced pin count test (RPCT) is becoming popular as a way of keeping down the cost of test for devices that are "fully loaded" with internal scan, BIST and 1149.1 boundary scan or JTAG. Companies such as IBM, Motorola and now Philips are using part of the boundary-scan register to access the low data-rate functional pins of a device in lieu of engaging these pins through a dedicated driver/sensor pin channel. High data-rate pins, such as Scan-In, *Scan-Out* and *Clock* pins are contacted directly. The boundary-scan register is designed to allow segments to be addressed through the TAP using private instructions, such as INTEST-RPCT. The addressed segment is used for serial-to-parallel access on the input side, and parallel-to-serial access on the output side. The remainder of the boundary-scan register is left in transparent mode.



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