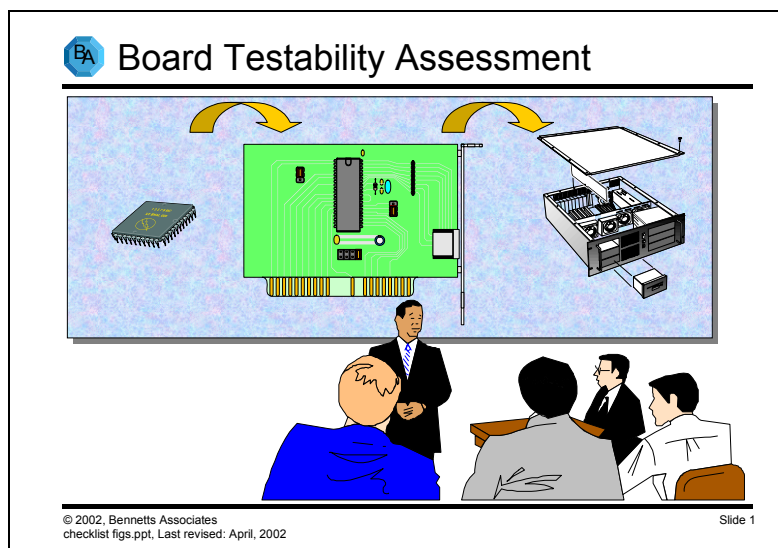


# Chip & Board Testability Assessment Checklist

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## Abstract:



This document summarizes a checklist of questions to assist testability assessment of a board mostly from a boundary-scan perspective but also from other test perspectives (ICT, FPT, AXI, AOI). The checklist is based on a set of Chip and Board Testability Guidelines, available from the author, also available on ASSET InterTech's web site, [www.asset-intertech.com](http://www.asset-intertech.com)

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**Before we get started.**

## 1. Before you start

<b>1.1 Data Requirements</b>	4
<p>Before you start, you will need:</p> <ul style="list-style-type: none"> <li>• Board level netlist</li> <li>• BSDL files for all 1149.1 devices and, if present, 1149.4, 1149.6 and 1532 devices</li> <li>• Cluster model files, also known as characteristic model files, containing IO and functional data for all non-boundary-scan devices</li> <li>• Board schematic</li> <li>• Data sheets for the devices on the board</li> <li>• Bill Of Materials (BOM)</li> <li>• A board</li> </ul>	
<b>1.2 Tester Availability and Tool Selection</b>	4
<p>What mix of tester types is available?</p> <ul style="list-style-type: none"> <li>• Boundary scan devices on board?</li> <li>• ICT: In-Circuit Test (multi-nail, fixed location)?</li> <li>• FPT: Flying Probe Test (few nails, movable location)?</li> <li>• AXI: Automated X-ray Inspection?</li> <li>• AOI: Automated Optical Inspection?</li> <li>• Emulation test?</li> </ul> <p>Tool selection</p> <ul style="list-style-type: none"> <li>• Does this design have any special features that should be considered when tools are selected?</li> <li>• Has a volume manufacturing test strategy been specified that could benefit from re-use of tests created during prototype debug?</li> <li>• Do the tools used for emulation, test, and In-System Configuration (ISC) support the scan path management device used?</li> </ul>	
<b>1.3 Checking Board Power-Up Sequence</b>	4
<p>Check the board power-up sequence</p> <ul style="list-style-type: none"> <li>• Does the board require a special power-up sequence e.g. different power-supply voltages applied in a certain sequence, or based on first loading a boot ROM? If so, is the sequence documented?</li> <li>• Does the board contain a master reset signal? Does this signal place all on-board devices into a known initialized safe state?</li> <li>• Are there any un-programmed PLDs or un-configured FPGAs on the board? If so, do these devices power-up in a safe state? And do devices that have access to un-programmed PLDs also power-up in a safe state?</li> <li>• Do boundary-scan devices power-up in the Test-Logic Reset state? (They should do if there is no TRST* signal but 1149.1 synthesis EDA vendors do not always comply with this requirement.)</li> </ul>	



**Now on to  
device checks**

## 2. On-Board Devices Checklist

<b>2.1 Identifying Boundary-Scan Devices</b>	4
Identify all 1149.1/1149.4/1149.6/1532 boundary scan devices <ul style="list-style-type: none"> <li>• SoCs</li> <li>• ASICs</li> <li>• Buffers</li> <li>• Off the shelf</li> <li>• Memory</li> <li>• Microprocessors</li> <li>• DSPs</li> <li>• PLDs</li> <li>• SERDES</li> <li>• ...</li> </ul>	
<b>2.2 Boundary-Scan Devices: Checking BSDL Files</b>	4
Check BSDL files for accuracy and correctness: <ul style="list-style-type: none"> <li>• What tests were made on the BSDL file (syntax, semantics, hardware verification tests) and how were the tests generated? Ask the vendor.             <ul style="list-style-type: none"> <li>• How did the vendor create the BSDL files – automatic creation or manual?</li> <li>• What level of the Standard applies: 1990, 1993 or 2001? (Check the <i>use</i> statement in the BSDL file for each device)</li> </ul> </li> <li>• Are there any known non-compliant features and are they identified? (They should be recorded in the Design Warnings section of the BSDL files. You might also want to check the data sheet.)</li> <li>• Are compliance-enable pins defined in the BSDL file? (There are examples where the compliance-enable pins exist but are not mentioned in the BSDL file.)</li> <li>• Check the need for and the presence of custom packages (“<i>use STD_1149_1_1994.all; use company_custom_package.all</i>”)</li> <li>• Is the maximum frequency for TCK defined? If so, is this a default value (cut and pasted from a template) or the actual value?</li> <li>• Does the device contain an analog section? If so, check to see if any boundary-scan cells exist between the digital and analog sections (not mandatory for 1149.1 mixed-signal devices unless the INTEST instruction is implemented).</li> <li>• Is there an audit trail for BSDL checking if the boundary-scan and /or the functional logic has been updated? Do device re-spins automatically cause an update to BSDL files? (Note: if the functional logic changes, the contents of the Identification register should also be updated. Often, it is not.) How are users notified of any BSDL changes?</li> <li>• What 1149.1 synthesis program was used? Is the program robust and proven?</li> <li>• Is there a central database of known problems with BSDL files? Have you checked the database?</li> <li>• Be especially careful of DSP devices. They are notorious for containing a variety of non-compliant features.</li> </ul>	
<b>2.3 Other Boundary-Scan Device Property Checks</b>	4
<ul style="list-style-type: none"> <li>• Are there any optional public instructions - IDCODE, USERCODE, INTEST, CLAMP, HIGHZ, RUNBIST?</li> <li>• For RUNBIST, is there information on how long the self-test will run and what the expected Pas/Fail result will look like?</li> <li>• Are there any private instructions? If so, is it clear what these instructions do? Can they be used at prototype-board debug? (Be careful. BSDL files contain only the minimum information about the behaviour of private instructions. Use private instructions with care.)</li> <li>• Does the device have the optional TRST* signal? If there is no TRST* pin, the device should automatically power-up in the Test-Logic Reset state. Does it do this?</li> </ul>	

<ul style="list-style-type: none"> <li>• What happens if two or more active outputs driving complementary logic values are shorted for any length of time? Is the resulting short-circuit current limited or can one active output drive against another active output and cause damage? If so, it is possible for damage to occur during interconnect test.</li> <li>• What are the power-up states of three-state outputs (they should be high-Z) and bidirectional signal pins (they should be inputs)? Note: this should happen in normal functional mode.</li> <li>• Can the status of three-state and bi-directs be controlled through boundary-scan cells or directly from the edge connector or via physical nails from an ICT or FPT tester?</li> <li>• Has the device been certified to be ground-bounce free when in worst-case EXTEST mode? (There should be no 1149.1-induced ground-bounce inside the device.)</li> <li>• At the physical level, are TAP pins placed physically next to each other or are they well-separated or positioned close to Not Connected (NC) pins? (They should be well separated or close to NC pins. Shorts between TDI and TDO can cause diagnostic problems.)</li> <li>• Are there any LVDS outputs or inputs? If so, are there boundary-scan cells on these pins and where are they placed? (See also section 3.17)</li> </ul>	
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<b>2.4 IEEE 1149.4 - Compliant Devices</b>		4
<p style="text-align: center;"><b><u>Note: the following questions are premature</u></b> <b><u>There are currently no commercial 1149.4 devices available.</u></b></p> <p>Are there any 1149.4 devices? If yes:</p> <ul style="list-style-type: none"> <li>• Is the device compliant to the IEEE 1149.4-1999 Standard, including the new PROBE instruction?</li> <li>• Does the BSDL file exist? Has it been checked for accuracy and correctness? Note: at the time of writing, BSDL extensions to cover 1149.4 features have not yet been approved by the 1149.4 Working Group.</li> <li>• Are any of the 1149.1 Digital Boundary Modules (DBMs) implemented as 1149.4 Analog Boundary Modules (ABMs)? (Using ABMs instead of DBMs enhances diagnostics at board level.)</li> <li>• Have DBMs been placed between the digital and analog cores (optional for 1149.4 devices unless INTEST is implemented)?</li> </ul>		

<b>2.5 IEEE 1149.6 - Compliant Devices</b>		4
<p style="text-align: center;"><b><u>Note: the following questions are premature but commercial 1149.6 devices are becoming available.</u></b></p> <p>Are there any 1149.6 devices? If yes:</p> <ul style="list-style-type: none"> <li>• Is the device compliant to the IEEE 1149.6-2003 Standard, including the new EXTEST-PULSE and EXTEST-TRAIN instructions?</li> <li>• Does the BSDL file exist? Has it been checked for accuracy and correctness?</li> <li>• Are the devices used on high-speed SERDES connections? If so, are the connections DC-coupled or AC-coupled? If AC-coupled, you will definitely need the new styles of 1149.6 boundary-scan transmitter and receiver scan cells.</li> </ul>		

<b>2.6 1532-Compliant Programmable Logic Devices</b>		4
<p style="text-align: center;"><b><u>Note: the following questions are premature in respect of 1532-compliant devices but 1532 is gaining in acceptance</u></b></p> <p>Are there Programmable Logic Devices (PLDs) on the board? If yes:</p> <ul style="list-style-type: none"> <li>• Are the devices compliant with the IEEE 1532-2002 Standard?</li> <li>• Do the BSDL files exist? Have they been checked for accuracy and correctness?</li> <li>• For 1532-compliant devices, what optional public instructions exist? (There are many in the 1532 Standard)</li> </ul>		

<ul style="list-style-type: none"> <li>For 1532-compliant devices, are there any special program security features? What are the implications on the ability to program and re-program the device once it's on the board?</li> </ul>	
<b>2.7 Other On-Board PLDs (Non-1532)</b>	
<ul style="list-style-type: none"> <li>If there are other non-1532-compliant PLDs on the board, will the devices be pre-programmed before they are placed on the board, or will they be programmed on the board? If on the board, will the device be programmed through the boundary-scan chain, or using an adjacent header?</li> <li>If the non-1532-compliant PLD is to be programmed on the board, what is the programming algorithm?</li> <li>Even if the non-1532-compliant PLD is programmed off the board, will it be verified on the board? If yes, do you have access to the device on the board?</li> </ul>	4
<b>2.8 On-Board Flash devices</b>	
<ul style="list-style-type: none"> <li>Are there flash devices on the board? If yes:</li> <li>Will the flash device be programmed: on the board or off the board?</li> <li>If on the board, do you know the programming algorithm? (See also section 3.15)</li> </ul>	4
<b>2.9 Checking Non-Boundary-Scan Devices: Availability of Cluster Model Data</b>	
<p>For non-boundary-scan devices:</p> <ul style="list-style-type: none"> <li>Do the IO cluster model data files exist? The files should contain information on pin IO type (I, O, OZ, IO); enable control pins and control values for OZ and IO pins; and whether the device can be made to behave transparently (pass-through mode).</li> <li>Does the device have a master Reset or Hold signal? If so, is it possible to control such signals during test operations?</li> </ul>	4
<ul style="list-style-type: none"> <li>Are there any discrete components? How are they characterized?</li> <li>Are there any analog components? How are they characterized?</li> </ul>	
<ul style="list-style-type: none"> <li>On future versions of this board, can any of the non-boundary-scan devices be changed for boundary-scan versions?</li> </ul>	
<p>For components (devices and discretes) that are not accessible from boundary-scan devices, can structural tests be carried out using other available tester types? For example:</p> <ul style="list-style-type: none"> <li>AOI to check for component presence (e.g. missing component, mis-aligned component), orientation (e.g. on an electrolytic capacitor), value (e.g. resistor markings, component identification marks) and bonding (e.g. quality of solder joint, sufficient solder, tombstone, gross shorts, lifted leads, bent leads).</li> <li>AXI to check primarily for solder quality (marginal joints, voids, excess solder, shorts, opens), also missing parts, mis-aligned parts</li> <li>In-Circuit Test or Flying Probe Test to check for dead part, wrong part, bad part, opens, shorts, functionally incorrect part</li> <li>Emulation test to check for functionally incorrect parts</li> </ul>	



**Now on to  
board checks**

### 3. Board-Level Checklist

3.1 Top-Level Board Scan-Chain Structure and TAP Access	4
<p>Primary scan chain:</p> <ul style="list-style-type: none"> <li>• What does the board top-level scan-chain look like: distribution of TCK, TMS and TRST* signals; TDO-to-TDI connects?</li> <li>• Can all primary TAP signals be accessed directly by the tester?</li> <li>• Do the primary TAP signals follow a standard layout - connector type, pin outs - and are they accessible even when the board is plugged into a motherboard (for use at system and field service test, also for in-system reconfiguration of PLDs and emulation tests)?</li> <li>• Can this chain be identified automatically? Are there branches based on multiplexers, jumpers, scan-path management devices (e.g. Scan Path Linkers/ScanBridge devices)? If muxed-based, is there direct tester access to the mux control lines?</li> <li>• Is the chain complete i.e. all the way from a primary TAP input to a primary TAP output?</li> <li>• Is the chain simple (single primary TAP) or complex (multiple primary TAPs)?</li> <li>• If multi-TAP, can the proposed tester handle multi-TAPs simultaneously?</li> <li>• Is there an earth connection at the primary TAP connector? (There should be.)</li> </ul>	
<p>Secondary scan chains:</p> <ul style="list-style-type: none"> <li>• Does the board contain any secondary scan chains, such as a detachable daughter board?</li> <li>• If so, is the primary scan chain broken if the daughter board is removed or is the chain reconfigurable through scan-path management devices such as Texas Instrument's Scan Path Linker or Linking Addressable Scan Port, National Semiconductor's ScanBridge, Firecron's JTS03, etc?</li> </ul>	
3.2 Master Boundary-Scan Control Signals: TCK	4
<p>For the TCK signal:</p> <ul style="list-style-type: none"> <li>• Is the TCK signal directly accessible from the edge-connector of the board?</li> <li>• Has the signal been distributed as if it were a critical clock – high speed, no crosstalk, etc? Note: these requirements are now mandated in some companies</li> <li>• Is the signal buffered? (It should be if drive load is greater than five devices, say.)</li> <li>• Is the signal inverted? (It should not be.)</li> <li>• Is the signal onto the board pulled to a safe state? (4.7 – 10 KOhm to POWER is typical.)</li> <li>• Does the signal need to be terminated to prevent reflections? (Series 68 ohms plus 100pF to GND is typical but some filters can affect the TCK slew rate and cause problems. If this happens, remove the capacitor to GND.)</li> <li>• What is the highest allowable frequency of TCK at the board level? Normally, the slowest boundary-scan device in the scan chain determines this frequency but watch out for slow rise and fall times on TCK signals. A spread of slew rates can also affect the maximum TCK frequency.</li> <li>• When TCK is not in use, is there a pull-up on the signal before distribution around the board? 10 KΩ is common.</li> </ul>	
3.3 Master Boundary-Scan Control Signals: TMS	4
<p>For the TMS signal:</p> <ul style="list-style-type: none"> <li>• Is the TMS signal directly accessible from the edge-connector of the board?</li> <li>• Has the signal been distributed so that, relative to TCK, TMS is stable while TCK is changing value 0-to-1?</li> <li>• Is the signal buffered? (It should be if drive load is greater than five devices, say.)</li> <li>• Is the signal inverted? (It should not be.)</li> <li>• Is the signal onto the board pulled to a safe state? (10 KΩ to POWER is typical)</li> </ul>	

<b>3.4 Master Boundary-Scan Control Signals: TDI</b>	4
<p>For the TDI signals:</p> <ul style="list-style-type: none"> <li>• Is the primary TDI signal into the TDI of the first device directly accessible from the edge-connector of the board?</li> <li>• Is the signal into the first device buffered? If not, should it be? (Normally, “yes”.)</li> <li>• Is the signal onto the board upstream of the buffer pulled to a safe state? (10 K<math>\Omega</math> to POWER is typical)</li> <li>• Sometimes, a series resistor is required in the chip-to-chip TDO-to-TDI connect to dampen reflections. It depends on the rise time of the TDI signal input.</li> </ul>	
<b>3.5 Master Boundary-Scan Control Signals: TDO</b>	4
<p>For the TDO signals:</p> <ul style="list-style-type: none"> <li>• Is the TDO signal from the TDO of the last device directly accessible from the edge-connector of the board?</li> <li>• Is the signal from the last device buffered off the board? (It should be if drive load is greater than 24mA, say.)</li> <li>• Does the signal off the board need to be terminated to prevent reflections?</li> </ul>	
<b>3.6 Master Boundary-Scan Control Signals: TRST*</b>	4
<p>For the TRST* signal:</p> <ul style="list-style-type: none"> <li>• Is the TRST* signal directly accessible from the edge-connector of the board?</li> <li>• Is the signal buffered? (It should be if drive load is greater than ten devices, say.)</li> <li>• Is the signal inverted? (It should not be.)</li> <li>• Is there a power-on reset circuit to ensure that the signal powers up low to start with (to reset the 1149.1 devices) but finishes up high (to reduce power consumption)? If not, does the signal have a tester-defeatable pull-down (10 K<math>\Omega</math> value) on the primary side of the buffer amplifier?</li> <li>• Is the TRST* signal activated when a system reset is applied? (This can be desirable when the board is working normally but make sure that the master reset signal is not used to hold devices in a safe state while boundary-scan testing is taking place.)</li> <li>• Note: if some boundary-scan devices have TRST* and others do not, then TRST* is useless for initializing all boundary-scan device. In which case, TRST*s should be pulled high during test mode (to allow normal boundary-scan operations on these devices) and low during functional mode (to hold these devices in their Test-Logic Reset state).</li> </ul>	
<b>3.7 Effects of Non-Compliance</b>	4
<p>Are there any suspected non-compliant 1149.1 devices on the board? (See section 2.2)</p> <ul style="list-style-type: none"> <li>• If so, is it possible to bypass the device physically e.g. by a jumper link from its TDI to its TDO?</li> <li>• Is it also possible to disconnect TMS from such a device using, for example, a series jumper or in-line switch? (This would prevent the device from responding to value changes on TMS.)</li> </ul>	
<b>3.8 Controlling Other Devices on the Board During Test</b>	4
<ul style="list-style-type: none"> <li>• For the non-boundary-scan devices on the board, are there any tied-off control pins for three-state or bidirectional signals? Can the pull-ups or pull-downs be defeated when in test mode, possibly with a real nail or from unused boundary-scan cells? Note: this is important if the three-state or bidirectional pins connect to a boundary-scan device with bidirectional BC_7s, or similar, scan cells.</li> <li>• Are there any on-board routines, such as Power On Self Test or Program-Boot, that can affect the correct operation of boundary-scan tests? If so, can the routines be controlled during boundary scan</li> </ul>	

test?	
<ul style="list-style-type: none"> <li>Are there any unused boundary-scan outputs e.g. from FPGA devices, that can be used to increase the controllability or observability of non-boundary-scan devices?</li> </ul>	

<b>3.9 Factors Affecting Successful Interconnect Test Using Boundary Scan</b>	<b>4</b>
<p>For each boundary-scan to non-boundary-scan interconnect, is there any risk of damage during EXTEST operation? In particular:</p> <ul style="list-style-type: none"> <li>Are there any first-level interactions between the boundary-scan and non-boundary-scan interfaces? Recall that any boundary-scan device in BYPASS mode is in its functional state, not test state. If some devices are required to be in BYPASS mode, it is usually better to do this using CLAMP or HIGHZ, so that the boundary-scan device outputs are in a known state. But check that important non-boundary-scan signals, such as Resets and Compliance-Enables are not affected by the values held on the boundary-scan cells of devices in CLAMP or HIGHZ modes. If the signals are affected, it might be better to use the BYPASS instruction to place the boundary-scan device in BYPASS mode.</li> <li>Are there any second level conflicts caused by the outputs of locally-controlled non-boundary-scan devices? For example, can RAM array outputs be driven into accidental bus conflict (contention)? If you have a tool that uses models to analyze second-level conflicts, check that the models define all the pins of the non-boundary-scan device, not just the inputs.</li> <li>Check for the presence of on-board lasers and, if present, turn them off in test mode. Note: some lasers, e.g. infra-red, are invisible to the human eye.</li> <li>Can all drivers of nets connected to both boundary-scan and non-boundary-scan devices be disabled via boundary-scan or physical nail control?</li> </ul>	
<p>Is there any risk of board-level ground bounce during worst-case EXTEST operation?</p> <ul style="list-style-type: none"> <li>Has this risk been assessed by the designer?</li> <li>If yes, can EXTEST be constrained by a Simultaneous Switching Output Limit (SSOL) on the tester and do you know what level of SSOL value to specify?</li> <li>Bi-directs may need a strong pull-down (circa 22 ohms) to reduce ground bounce possibilities</li> </ul>	
<ul style="list-style-type: none"> <li>Do any of the on-board boundary-scan devices contain internal DFT structures e.g. internal scan paths, memory BIST or logic BIST, accessible through the device TAP using private instructions? If so, is there value in re-using these structures at board level to support board-level diagnostics?</li> </ul>	
<ul style="list-style-type: none"> <li>Are there any boundary scan devices connected directly to an edge connector? If so, can a passive or active loop-back test be used to check for opens between the scan cells and the connector pins? Alternatively, can you plug in a dummy 1149.1 device for testing purposes?</li> <li>Effect of noise and crosstalk. Interconnect tests place values on nets that can be very different to normal functional values. As a result, crosstalk or noise under test conditions can cause false fails.</li> </ul>	
<ul style="list-style-type: none"> <li>Does the board contain a mix of different-voltage-level boundary-scan devices? If so, are appropriate voltage converters placed on the TCK, TMS and TDO-to-TDI interconnects so that interconnect tests can be applied between the different-voltage-level devices?</li> </ul>	

<b>3.10 Testing Non-Boundary-Scan Memory Devices via Boundary Scan</b>	<b>4</b>
<p>How will non-boundary-scan memory devices be tested?</p> <ul style="list-style-type: none"> <li>Are the Data, Address and Control signals accessible from a boundary-scan interface?</li> <li>Can devices that normally access Data, Address and Control signals be disabled to allow alternative access from a boundary-scan device?</li> <li>If not, is there an on-board processor that can be used as a tester?</li> <li>Are suitable functional models for the behavior of the RAM devices available for automatic memory test-pattern generation?</li> <li>For DDRAMs and SDRAMs, is the Write/Read cycle time less than the refresh time? Does the tool calculate these times?</li> </ul>	

<ul style="list-style-type: none"> <li>• Are any of the RAMs under the control of a free-running RAM clock (not TCK)? If so, are there any problems to do with the asynchronous relationship between the RAM clock and TCK e.g. synchronizing between boundary-scan operations and RAM operations?</li> <li>• Can any free-running clocks to the RAM devices be controlled e.g. through the Select pins of a PLL?</li> <li>• In test mode, is there any risk of contention (bus conflict) on the Data Bus?</li> </ul>	
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<b>3.11 Testing Other Non-Boundary-Scan Devices via Boundary Scan</b>	<b>4</b>
<p>How will non-boundary-scan non-memory devices be tested?</p> <ul style="list-style-type: none"> <li>• What type of device is it – simple pass-thru e.g. line drivers, or more complex MSI device?</li> <li>• What access is there to the non-boundary-scan device? <ul style="list-style-type: none"> <li>• From boundary-scan devices?</li> <li>• From an edge connector, or equivalent?</li> <li>• Through in-circuit nails? (See section 3.12, also section 2.9)</li> <li>• Through non-electrical test techniques e.g. AXI or AOI? (See section 2.9)</li> </ul> </li> <li>• Are there any non-boundary-scan device inputs that are not directly controllable or outputs that are not directly observable?</li> <li>• What tests will be applied?</li> <li>• What is the purpose of these tests? Structural or functional checkout?</li> <li>• Where did the tests come from? ATPG tools (e.g. on an ICT), manual?</li> <li>• What is the state of surrounding non-participating non-boundary-scan devices during a specific cluster test? Can the non-participating devices interfere with the tests and, if so, can their outputs be held in a non-interfering state? Ideally, use HIGHZ or CLAMP, else BYPASS. Using EXTEST will place considerably more boundary-scan cells in the chain thereby increasing the test time.</li> </ul>	

<b>3.12 Testing Non-Boundary-Scan Devices via Boundary Scan and/or Real Nails/AXI/AOI</b>	<b>4</b>
<p>Will the board be tested with a mix of real nails (from an In-Circuit Tester or Flying Probe Tester) and virtual nails (boundary-scan cells)? If yes:</p> <ul style="list-style-type: none"> <li>• Have the real nails been placed to maximize the controllability and observability into the non-boundary-scan devices?</li> <li>• Where do the cluster tests come from? The ICT library?</li> <li>• Are the tests in an importable format?</li> <li>• What is the purpose of the tests? Structural or functional checkout?</li> <li>• Is there a need to synchronize the tests if they are partly applied through the real nails and partly through the virtual nails? If yes, will synchronization be achievable?</li> <li>• Have nails been placed on TDO-to-TDI interconnects to simplify the diagnosis of opens on these interconnects?</li> <li>• In future versions of the board, are there hidden nets that would benefit from board-surface test lands for physical probing? Note: two approaches: <ul style="list-style-type: none"> <li>• Test Point Removal: make all nets probable by default and remove all those that do not require a physical probe test land</li> <li>• Test Point Insertion: make no nets probable by default and add probe points based on inability to control/observe through boundary-scan cells</li> </ul> </li> </ul>	

<b>3.13 In-System Configuration of PLDs</b>	<b>4</b>
<p>Does the board contain PLDs?</p> <ul style="list-style-type: none"> <li>• If so, are they 1532 compliant and included in the board scan chain?</li> <li>• If not, is there a need to configure or re-configure the PLDs once they are on the board?</li> <li>• If yes, how will this be achieved: via a header, through the boundary-scan chain, via ICT/FPT nails?</li> <li>• If compliance-enable pins exist, are the pins directly controllable by the tester? If the compliance-enable pins are coming from another boundary-scan device, is this device upstream or downstream of the CPLD. If downstream, it may be impossible to access the boundary-scan device – a “chicken and</li> </ul>	

<p>egg” problem.</p> <ul style="list-style-type: none"> <li>• Are the configuration files suitable for on-board configuration through the boundary-scan chain?</li> <li>• For on-board PLDs, are the compliance-enable pins directly accessible or are they tied to their enable levels through defeatable weak pull-ups or weak pull-downs as appropriate? (External test access control is preferred over boundary scan control.)</li> </ul>	
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<b>3.14 In-System Configuration of FPGAs</b>		4
<p>Does the board contain FPGAs?</p> <ul style="list-style-type: none"> <li>• If so, are all the configuration modes e.g. slave-serial, master-serial, boundary scan, explained in the accompanying documentation? And are all modes required once the device is on the board? Note: this will usually require direct access (from boundary-scan cells or adjacent header or physical nails) to all FPGA master mode control signals e.g. PROG pins.</li> <li>• Check how much data is required to configure the FPGA and calculate the data delivery time using the modes that are available to you.</li> <li>• If the FPGA contains internal processor cores accessible through a JTAG port, be aware that “JTAG” does not necessarily mean 1149.1-compliant.</li> <li>• Check that JTAG port signals brought out to pins are not tied to 1149.1 TAP signals.</li> <li>• For configuration, check (a) is the serial PROM an 1149.1 device and in the board-level scan chain or (b) is the FPGA an 1149.1 device and in the scan chain? What is the exact configuration sequence?</li> <li>• If the FPGA is already configured, check that the BSDL file has been appropriately updated to reflect post-configuration behaviour e.g. name change, new private instructions, USERCODE values, etc.</li> <li>• If the device is not configured, can this be checked to confirm? (Usually done by executing the USERCODE instruction or checking the higher-order IR capture bits.)</li> <li>• Check the contents of the Design-Warning section in the BSDL file.</li> <li>• Beware of different drive/sense voltage settings on output banks (3.3v LVTTTL, 3.3/2.5/1.8/1.5v LVCMOS, LVDS, etc)</li> <li>• For pre-configured FPGAs, check that there is no risk of losing the configuration caused by any form of test activity (through boundary-scan cells or physical nails).</li> </ul>		

<b>3.15 In-System Configuration of Flash Devices</b>		4
<p>Does the board contain Flash devices?</p> <ul style="list-style-type: none"> <li>• If so, are the Data, Address and Control signals accessible from the boundary-scan devices or via the nails of an ICT/FPT tester for the purpose of programming?</li> <li>• If not, is there a need to program the Flash devices once they are on the board? If yes, how will this be achieved?</li> <li>• Have you assessed the time it will take to program the flash device? Is this time acceptable?</li> <li>• Are there any limits on the frequency of TCK caused by slow devices in the chain?</li> <li>• If yes, would a Texas Instruments Scan-Path Linker, or similar, help? Or can slow devices be bypassed with jumpers?</li> <li>• Can all non-scan outputs that share a flash bus be disabled during flash programming?</li> </ul>		

<b>3.16 On-Board DSP and Microprocessor Devices: Need for Emulation</b>		4
<p>Does the board contain DSP or Microprocessor devices and, if so, is there a need to emulate these devices for design debug or even for supplementary structural tests?</p> <ul style="list-style-type: none"> <li>• If yes, can the devices be isolated from other devices or can the emulation be carried out with other connected devices active?</li> <li>• If the emulated device must be isolated, how is this achieved? By using a TI Scan Path Linker, or similar, or by an adjacent header? (Watch out for mode pins that need to be in one state for emulation but another state for 1149.1 compliance.)</li> </ul>		

<b>3.17 Existence of On-Board DC or AC Low-Voltage Differential Signaling (LVDS)</b>	4
<ul style="list-style-type: none"> <li>Does the board contain high-speed (GBps frequencies) DC-coupled or AC-coupled Low-Voltage Differential Signals? If so, these interconnects require special attention and need to be tested using 1149.6 or IBIST styles of solution. Contact the author at <a href="mailto:ben@dft.co.uk">ben@dft.co.uk</a> for more information on these techniques.</li> </ul>	
<b>3.18 Miscellaneous</b>	4
<ul style="list-style-type: none"> <li>Can system clock signals be disabled by boundary-scan control during board test?</li> </ul>	

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### About the Author



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Previously, he has worked for LogicVision, Synopsys, GenRad and Cirrus Computers. Between 1986 and 1993, he was a free-lance consultant and lecturer on Design-for-Test (DFT) topics. During this time, he was a member of JTAG, the organization that created the IEEE 1149.1 Boundary-Scan Standard. He is an Advisor to the Board of Directors of ASSET InterTech Inc. and a member of the Technical Advisory Board of Teseda Inc.

Ben has published over 100 papers plus three books on test and DFT subjects.