

## BOUNDARY SCAN DIAGNOSTIC & REPAIR STATION

### PRODUCT OVERVIEW

ScanWorks Diagnostic & Repair Station provides all the features necessary to quickly and easily diagnose and repair defects detected on boards during manufacturing. A separate repair station allows your development and manufacturing operations to continue uninterrupted while boards are repaired off-line. The Diagnostic & Repair Station provides access to the built-in debug features of each test type but restricts the ability to modify designs or regenerate ScanWorks tests, protecting the integrity of the ScanWorks projects. Several of the major benefits of the Diagnostic & Repair Station are:

- Project Management — Import and run the same tests used in manufacturing, using either the ScanWorks sequencer or a custom user interface
- Comprehensive test application — Apply and

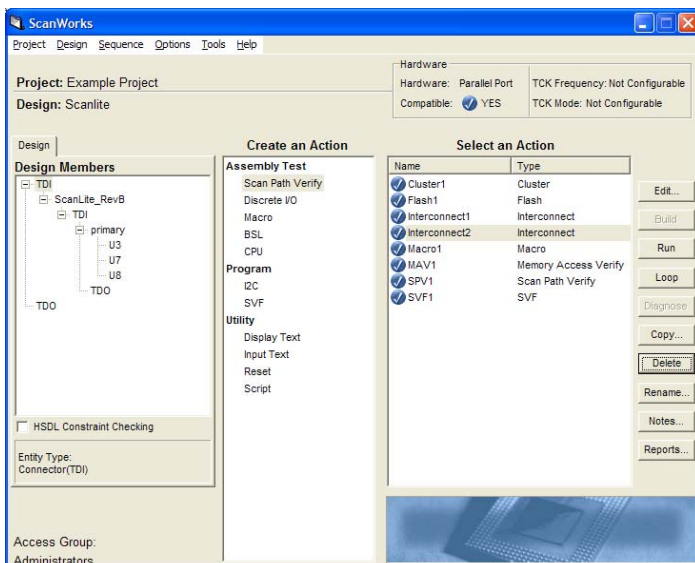
diagnose any test created with an Test Development Station, including PLD and flash memory programming

- Consistent, intuitive user interface — Uses the same basic user interface as the Test Development Station
- Maintain test integrity — By limiting access to test generation tools, you maintain safety of test and are assured the same tests are used for debug as were used for detection in manufacturing
- Quick defect isolation with pin-level diagnostics for interconnect test — Pin-level diagnostics to isolate a defect to the most likely device pin are included
- Graphical views of the board layout and schematic are linked directly from the fault reports, enabling you to quickly pin point the most likely location of the defect.

Diagnostic & Repair Station includes features like the design manager, scan path verification, pin-level diagnostics for interconnect tests, test results windows for each test type, graphical fault highlighting, and the test sequencer. You also have access to the interactive debugger and scan analyzer, and macros to create custom tests to control and observe specific device pins to isolate defects.

### DESIGN MANAGEMENT

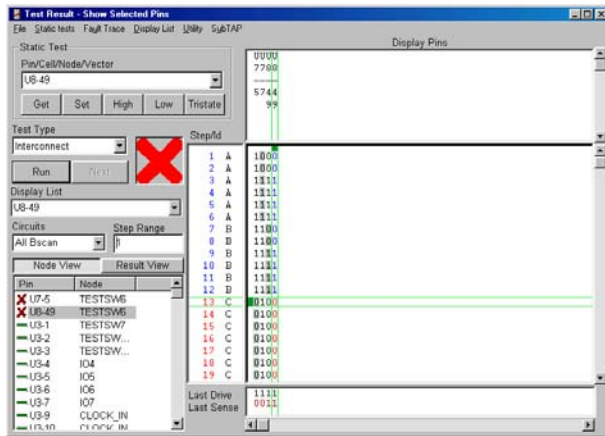
ScanWorks design management provides features needed to link your Diagnostic and Repair Station with a Test Development Station or a Manufacturing Station. The design management software features allow you to:





## INTERCONNECT TEST DIAGNOSTICS

Interconnect test diagnostic tools includes net and pin level diagnostic reports and a built-in test results



dialog. The diagnostic report provides all the information available about any net on which an unexpected response is detected, including the most likely type of defect, (open or shorted) and the device and pin information about all other connections to the net.

The test results dialog provides a state table view of the results of applying interconnect tests. Each scan operation is shown for selected pins or nets, enabling you see exactly what conditions lead to miscompares. Miscompares are highlighted and the driving pins are clearly indicated. You can rerun the tests from within

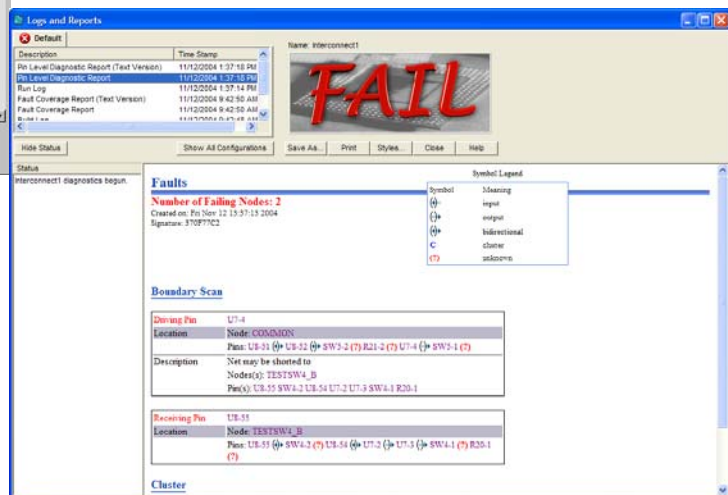
## MEMORY ACCESS VERIFICATION DIAGNOSTICS

Tests created with the Memory Access Verification tool can detect defects on data, address and control signals connected between boundary-scan device and non-boundary-scan memory devices. Defects can be diagnosed to the data or address signal, and in some cases to a specific control signal. A diagnostic report that indicates the signal and the specific memory pin involved is generated. Pins are linked to the board

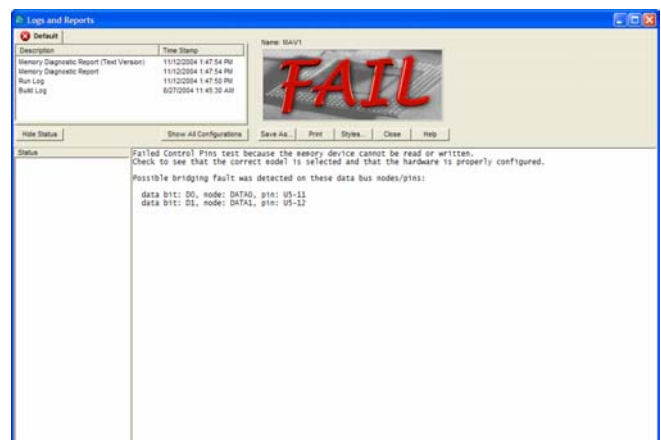
the test results dialog and also observe specific pins or set them to specific logic levels.

## INTERCONNECT PIN-LEVEL DIAGNOSTICS

The Diagnostic & Repair Station include diagnostics to the pin level for interconnect tests. The report generated provides the type of fault detected, the most likely source of the fault, information about the net to which the pin is connected, and links to



specific nets or pins in the InterComm Design Browser layout view. The report indicates the type of connection for each pin on the net using symbols to indicate input, output, or bi-directional and if the device is a cluster (non-boundary-scan), or unknown.



layout view provided by the Graphical Fault Highlighting feature, making it easy to locate the suspected pin on the actual board being tested.

A test results dialog is also provided. Like the interconnect debugger, it provides a state table view of the scan operations needed to execute the read/write operations necessary to complete the test. Data is displayed in two modes: A cycle mode that shows only the significant scans for reading and writing to the memory and a vector mode that shows every scan.

## MACRO LANGUAGE

The macro programming language provided with a Diagnostic & Repair Station is a powerful, high-level language that provides access to the design at any level; from individual scan cells to entire test registers or subsets of test registers. With specialized functions and procedures you can control or observe a specific pin or create a complete test for a cluster of non-boundary-scan logic. With a macro program you can establish “safe” conditions before entering the boundary-scan test mode or maintain a safe state throughout testing.

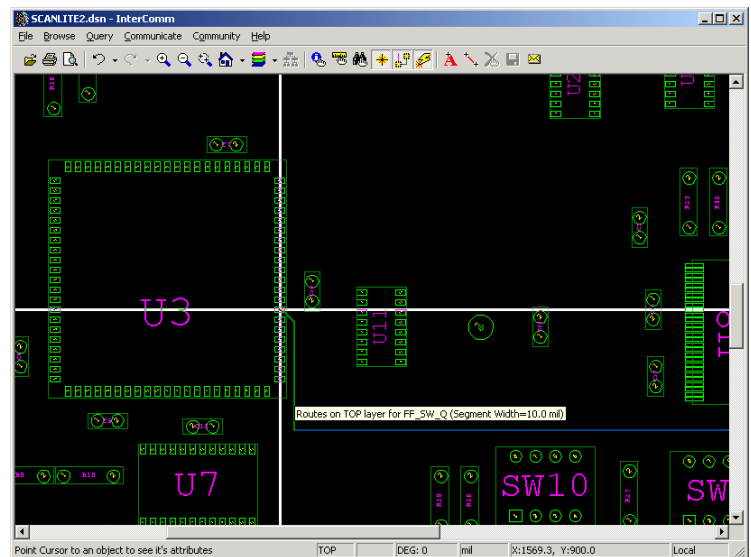
## PROCESS AUTOMATION SCRIPTING API

Process Automation Scripting is a very powerful tool with many applications. It supports custom test generation by providing access to all of the boundary scan features on any device that is accessible to ScanWorks. Test patterns can be applied and the results observed at any level of the design, from specific scan cells to nets at the board or system level. Any test programming language can be used to create these tests, including languages that supports Microsoft’s Component Object Model (COM), Tcl, Perl, Visual Basic, C, C# and C++. Process

Automation Scripting is especially useful during prototype debug and board repair with a Diagnostic & Repair Station because it enables you to control the state of the UUT while probing with traditional test instruments such as volt meters, oscilloscopes, and logic analyzers. You can set static values on pins or create loop tests to toggle pins while tracing them on the board. And it can all be done using your favorite test programming language.

## GRAPHICAL FAULT HIGHLIGHTING

The Graphical Fault Highlighting feature gives you access to a graphical view of the board layout using the powerful InterComm Design Browser from PTC (formerly OHIO Design). Interconnect test and Memory Access Verification test reports are linked to the layout view by clicking on a pin or net in the report. Cross hairs pinpoint the location of the pin or



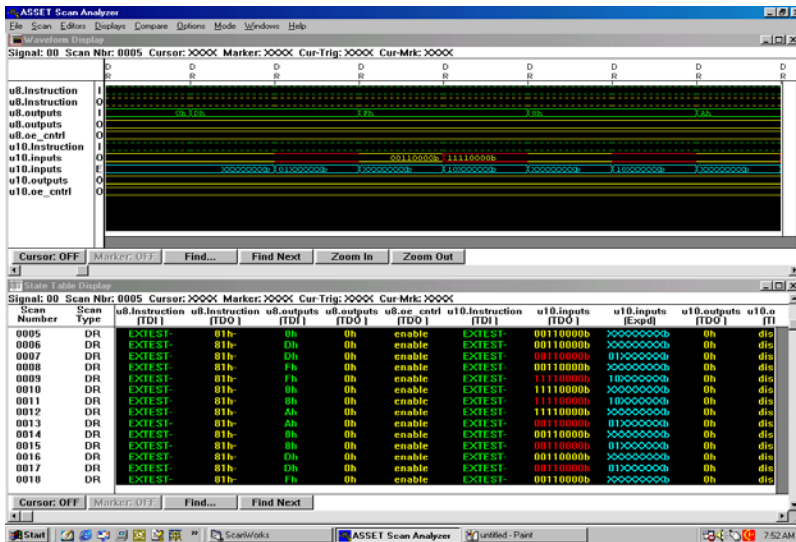
net in the layout view where the Design Browser gives you access to all the available information about that pin, and shows you the exact routing of the net connected to that pin. You can easily locate the suspected pin on the actual board being tested and quickly inspect it for obvious defects. You can cross-

highlight the layout view to a schematic view to see the functional logic associated with the pin. The InterComm Design Browser is provided by PTC. Additional information about the InterComm Design Browser is available at: [InterComm on PTC Web Site](http://www.ptc.com/intercomm)

## INTERACTIVE DEBUGGER/SCAN ANALYZER

The Debugger/Scan Analyzer feature gives you powerful tools to debug tests created with macros or as SVF files. The debugger gives you access to boundary-scan cells and registers, from the device, board or system level. You control when the scan operations occur, the values shifted in and can observe the results shifted out in either a register view or a pin view. You can single-step macro

programs or SVF files to see the results of each scan. The Scan Analyzer provides either a waveform or a state table view of the execution of a macro program or SVF file. Any mismatches are highlighted, enabling you to see exactly what lead up to the mismatches.



### Highlights

- Apply and diagnose defects detected by manufacturing tests
- Test can be applied interactively, by using the ScanWorks Sequencer, or by using custom user interfaces created for manufacturing with ScanWorks APIs.
- Includes access to built-in tools to isolate faults for scan path verification, interconnect test, memory access verification, and flash programming.
- Graphical fault highlighting pinpoints detected faults on a graphical view of the board layout.
- Debugger/scan analyzer and macros provide more