

## INTEL® XDP ADAPTER CONFIGURATION

This application note explains how to connect Processor-Controlled Test (PCT) 3040 test and debug solutions to a board that provides an Intel® eXtended Debug Port (XDP) for access to the processor's debug port (Figure 1 below). For further details on the XDP, please refer to the Intel® document "Debug Port Design Guide for UP/DP Systems" at the following location:

<http://download.intel.com/design/Pentium4/guides/31337301.pdf>

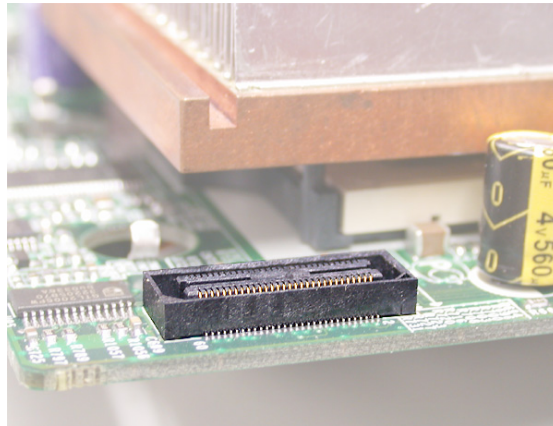


Figure 1. Intel® XDP port (60 pins)

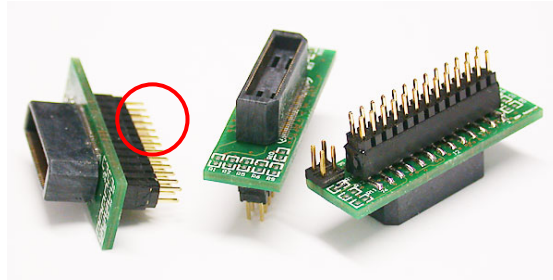
The 60-pin Intel® XDP provides connections for up to 4 "Observation and Control Ports", each consisting of 6 signal lines. These were previously termed "Breakpoint Monitor" signals, hence the 6 active-low signal lines for each port are denoted as BPM[5:0]#.

PCT 3040 solutions must be connected to processor debug ports via an Intel-specific Debug Port Adapter (DPA). We originally designed the PCT DPA shown in Figure 2 for connection to 26-pin Intel® ITP700 ports.



Figure 2. Debug Port Adapter (DPA)

The XDP Adapter shown in Figure 3 converts the 26-pin connector on the DPA to a 60-pin connector for insertion into a board's XDP.



*Figure 3. XDP Adapter – red circle shows the location of the version number*

The DPA only provides connections for one set of BPM[5:0]# lines. However, where more than one of the 4 BPM ports in the XDP is routed to a different processor in a multi-processor (MP) system, the corresponding BPM lines from each processor can be connected together (wire-OR). This connection is carried out by the addition of resistors to the XDP Adapter. The PCT 3040 test interface is then able to communicate fully with each processor.

### **XDP ADAPTER VERSIONS**

There are currently 2 versions of the XDP Adapter, the later version having superseded the earlier one:

8000-45022F-002  
8000-45022F-003 (supersedes version 002)

These part numbers are printed in the copper layer of the XDP Adapter, in the location shown by the red circle in Figure 3. This text is very small – a magnifying glass may be required to read it! An easier way to identify the version is to compare the bottom overlays shown in Figures 5 and 7 on the following page – there are more resistor locations on the adapter version 003.

The difference between versions 002 and 003 is the way in which the 4 BMP ports are wired together by default.

Version 002 was configured so that BPM ports **a** and **b** were permanently linked, and the remaining ports (**c** & **d**) could also be linked by inserting appropriate 0R resistors – see Table 1 below.

<b>Lines</b>	<b>Insert Resistors</b>	<b>Comment</b>
BPM[5:0]a	N/A	Permanently linked to DPA
BPM[5:0]b	N/A	Permanently linked to DPA
BPM[5:0]c	R1, R3, R5, R7, R9, R11	Optional
BPM[5:0]d	R2, R4, R6, R8, R10, R12	Optional
V <sub>TT</sub> Power Source	R15 (XDP pin 43) R18 (XDP pin 44)	Normally only R15 required
TCK0	R13	Mandatory
TCK1	R14	For use with IBIST DPA only

Table 1. XDP Adapter Version 002 – optional links by adding 0R resistors

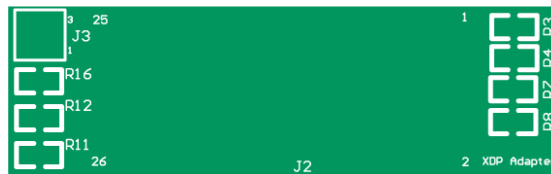


Figure 4. Version 002 Top Overlay



Figure 5. Version 002 Bottom Overlay

Version 003 is configured with only port **a** permanently connected, and the remaining ports (**b**, **c** & **d**) can be individually linked by adding 0R resistors – see Table 2. The reason for making all links optional except for port **a** in the 003 version is that on some boards the BPM ports may be routed to other components such as the Memory Controller Hub (MCH). Linking MCH and processor signals would present a potential conflict.

Lines	Insert Resistors	Comment
BPM[5:0]a	N/A	Permanently linked to DPA
BPM[5:0]b	R19, R20, R21, R22, R23, R24	Optional
BPM[5:0]c	R1, R3, R5, R7, R9, R11	Optional
BPM[5:0]d	R2, R4, R6, R8, R10, R12	Optional
V <sub>TT</sub> Power Source	R15 (XDP pin 43)	Normally only R15 required
	R18 (XDP pin 44)	
TCK0	R13	Mandatory
TCK1	R14	For use with IBIST DPA only

Table 2. XDP Adapter Version 003 – optional links by adding OR resistors

**Note:** In the very unlikely event that a system has been designed with BPM port a routed to the MCH for example, then neither version of the adapter will work, as port a cannot be isolated.

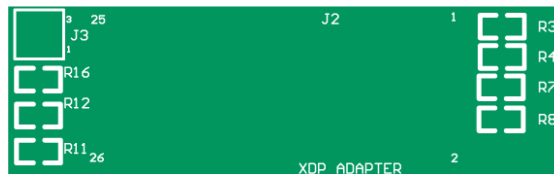


Figure 6. Version 003 Top Overlay



Figure 7. Version 003 Bottom Overlay

## V<sub>TT</sub> CONNECTIONS

The V<sub>TT</sub> source is normally derived from pin 43 on the platform XDP header (with R15 inserted), however if necessary pin 44 may be used instead.

## TCK CONNECTIONS

Tables 1 and 2 also describe the configuration necessary to use the second TCK source (TCK1). This is only applicable when using recent IBIST-compatible DPAs. While identification is not possible from the external casing shown in Figure 2, the internal DPA board overlay indicates IBIST compatibility, as shown in Figure 9.

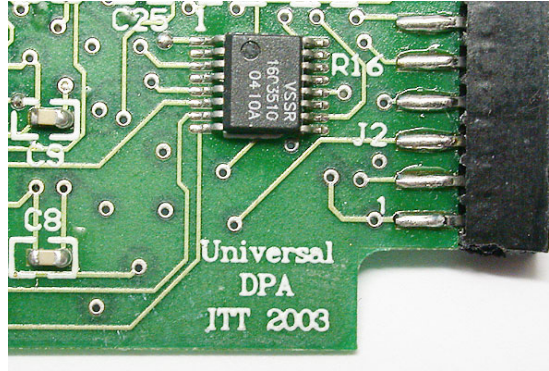


Figure 8. Non-IBIST DPA

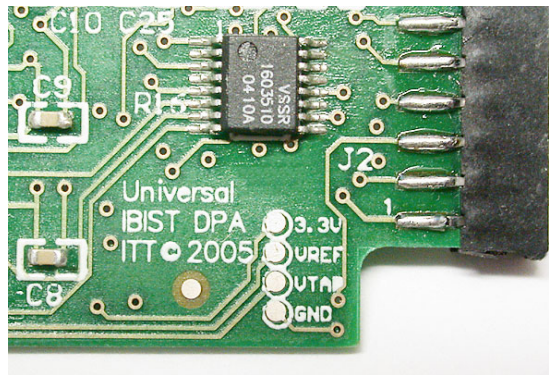


Figure 8. IBIST-compatible DPA

### CONTACTS FOR ADDITIONAL INFORMATION

For contact details of our worldwide reps. please see our website: <http://www.asset-intertech.com/contact.html>