Status Report: ASSET Boundary-Scan Test

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Background:

As contract manufacturers in the electronics industry we are forced to monitor quality through active testing. Good overall test strategies result in good product going out to the customer. Yet while test is fundamental to manufacturing, there are several factors that limit test development and integration. Faced with fixturing and tooling costs, development lead times, relatively short product life spans, and limited test access we often find that there is reluctance towards investment in effective distributed test strategies that include in-circuit, functional, and system level testing. Gaps in testing lead to gaps in defect detection and repair, both of which invariably lead to higher manufacturing costs and lower on-time deliveries.

To simplify the complex problem of testing boards and systems for a range of manufacturing defects, Reptron—Hibbing has recently invested in ScanWorks. This software tool, developed by *ASSET InterTech*, provides the means for automated in-circuit and functional level testing of circuit boards that incorporate boundary-scan devices.

Boundary-Scan:

Boundary-Scan is a method of testing boards that contain integrated circuits that comply with the IEEE 1149.1 specification. In a boundary-scan device, each digital primary input signal and primary output signal is supplemented with a multi-purpose memory element called a boundary-scan cell. These scan cells act as drivers and receivers that run independently from the internal logic of a given device.

Because boundary-scan cells can be arbitrarily programmed to be in known states, boundary-scan testing provides the ability to set up and apply tests across the interconnect structures on a circuit board. Essentially, boundary-scan testing works by driving test vectors from one boundary-scan device and then sensing the response to these vectors on another boundary scan device. There are several fundamental benefits to boundary-scan testing:

- All test interfacing is accomplished using only four JTAG signals: TCK, TMS, TDI, and TDO. As a result, fixturing costs are minimal.
- Boundary-scan devices have the capability of controlling non-boundary scan devices, thereby increasing test coverage across the PCB.
- Faults may be diagnosed right down to pin level failures.
- Board functionality is tested without having to configure microprocessors, ASICs, or programmable logic (such as FPGAs). There are many situations where a board will freeze during the boot process rendering other forms of functional test useless.
- Boundary scan can program static memory such as flash.

How Boundary-Scan Test is Implemented:

ScanWorks relies on a thorough design description to model the hardware to be tested. The design description requirements are similar to what is commonly used for developing in-circuit tests.

These include:

- Boundary Scan Description Language (BSDL) files that describe the individual boundary-scan devices on the circuit board.
- A description of the interconnections between the boundary-scan devices.
- Descriptions of all board level interconnects using netlists or standard PCB layout files.
- Descriptions of non-boundary-scan devices used in the design.
- Descriptions of power and ground nets in the design.

Once all of the design requirements are thoroughly debugged and verified, they are then imported into ScanWorks and built into a hierarchical design description of the hardware to be tested. Once this level of design description exists, it is then possible to automatically create and apply tests at the device, board, and system levels.

The automated test generators are very effective at developing intrinsically safe test vectors for boundary-scan devices. There are also device libraries, as well as modeling and debug tools that can be used for increasing test coverage by developing tests for non-boundary-scan devices. While modeling non-boundary-scan devices is an effective way to increase testability, it should be noted that this additional coverage comes at a cost in terms of model development and debugging time. Once tests are developed, however, software operation is very straightforward: it is simply a matter of clicking on a desired test or group of tests. As a result, training technicians to understand and use this tool can be accomplished in a few hours.

The Test Interface:

To electrically connect to the four JTAG signals, ScanWorks requires that a simple header be connected to the unit under test (UUT). The simplest method is to use a fixture with test probes that bring the JTAG signals directly to nets on the UUT.

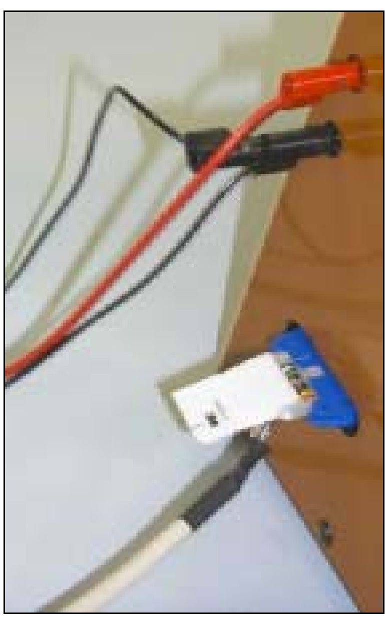


Figure 1

Figure 1 demonstrates the required header needed to interface the JTAG signals TCK, TMS, TDI, and TDO to the UUT. The cable coming into the side of the test fixture is broken out and wired directly to test probes that contact the UUT. Additionally, all power supply and JTAG grounds must be wired in common.

As has been mentioned earlier, there is a distinct advantage to boundary-scan testing in terms of associated fixturing costs. *Figure 2* demonstrates the degree of fixturing required to access a circuit board with approximately 1400 nets using boundary-scan access. *Figure 3* shows an in-circuit test fixture for a circuit board with an equivalent net count.

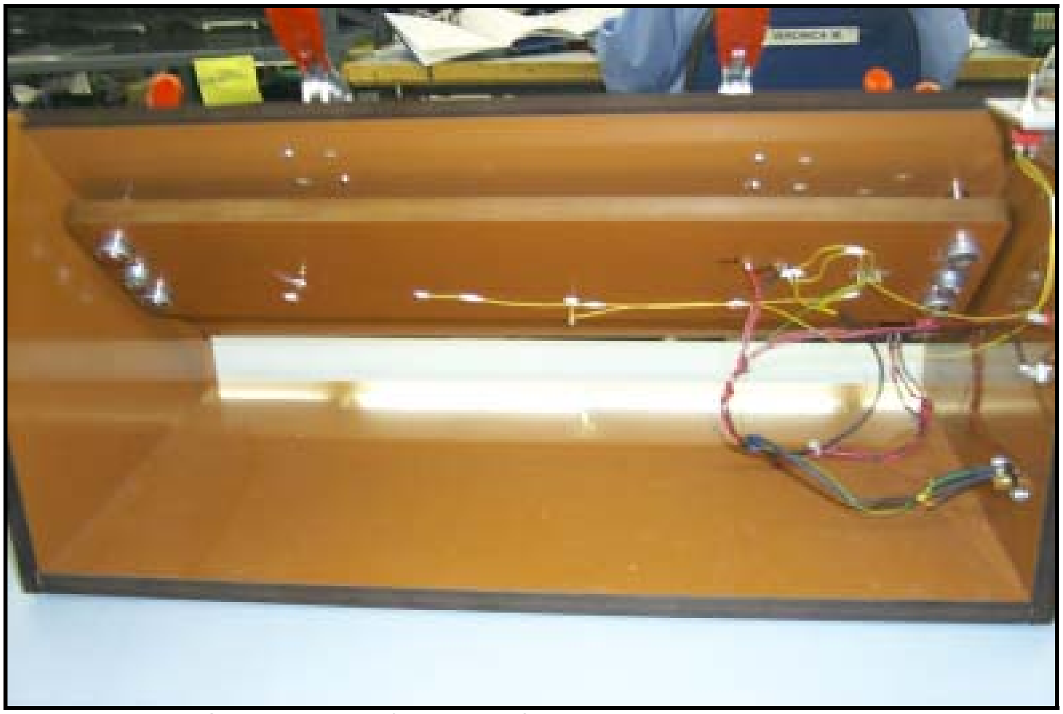


Figure 2: Boundary Scan Test Fixture for 1400 Net Circuit Board

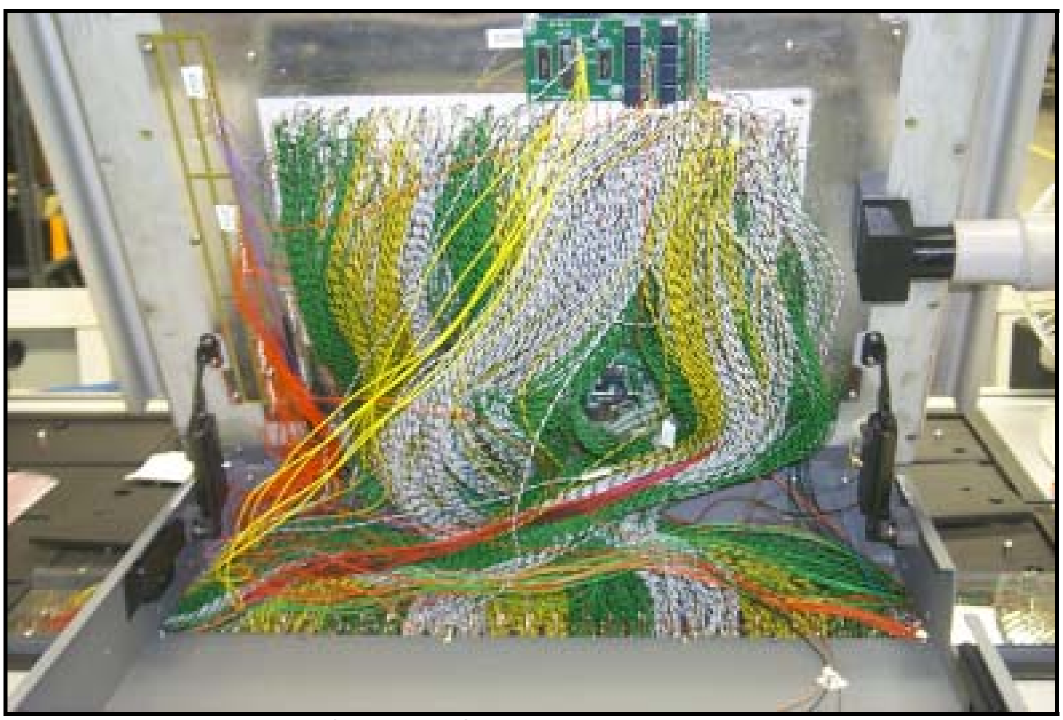


Figure 3: In-circuit Test Fixture for 1400 Net Circuit Board

Test Case Number One:

One of our customers, Eastern Research, designs and markets high-speed digital networking and telecom switching equipment. Their product line is diverse, product life span is short, and design-to-market times are rapid. For new products, as well as for low-volume products, there is usually only a functional or system level test with very limited diagnostic capability. As a result, we have been faced with significant troubleshooting costs associated with repairing defective product and holding back shipments. To combat these costs we have applied ScanWorks towards diagnosing and troubleshooting problem boards.

We elected to develop our first test for a product called the DNX-1U. This circuit board has three boundary scan devices: a Motorola 68360 microprocessor, a Xilinx CPLD, and a Xilinx FPGA. Because the devices were not designed as a single scan chain, it was necessary to build a simple fixture that would tie all four of the JTAG signals together (see *Figure 4*). Ten test points were required to enforce the scan chain and to interface to the JTAG connector from the test equipment (refer back to *Figure 2*).

Figure 4: DNX-1U Tester Configuration

We started with a program developed by *ASSET InterTech* that tested the basic functionality of the boundary scan devices as well as digital level board interconnects. This level of test provided approximately 30% coverage of board faults. Looking at the nature of the board level failures we were seeing, we realized that we were lacking test coverage in several critical areas.

As our literacy with the software increased, we added more refined testing and functionality to our boundary-scan program. This included:

- Flash memory testing and programming capability
- Full cell DRAM testing
- RS232 loopback port testing
- RS530/V.35 high speed port loopback testing
- Peripheral line alarm loopback testing
- Relay contact closure testing
- E1/T1 feedthrough testing (using external I/O)

Much of the functionality of the above tests was accomplished by modeling non-boundary scan devices so that these parts can be driven and then sensed by the primary boundary scan devices. This technique—called 'cluster testing'—is a very powerful tool in that it allowed us to test the board on a functional level while still maintaining complete pin level diagnostic capability. Further, it allowed us to increase board fault test coverage from 30% to approximately 70%.

Test Case Number Two:

For our second test case we selected a board called the DNX-50301. This circuit board has a total of thirteen boundary-scan devices and was selected because it is representative of one of the more complex digital designs for which boundary-scan testing is possible. Out of 1775 nets present on the PCB, 1283 nets were directly connected to boundary-scan devices. This amount of coverage (approximately 72%) suggested that not only could we get a good test for the DNX-50301 assembly, but that we could also test out the robustness of the ScanWorks development software.

Figure 5: DNX-50301 Tester Configuration

The DNX-50301 has a Motorola 68360 processor, four PMC-Sierra high-speed framing chips, four Xilinx FPGAs, two Xilinx CPLDs, and two Xilinx flash chips. The first step in this test development was to map out the scan chain. A scan chain simply implies that the serial output pin of one boundary-scan device connects to the serial input pin of the next. This TDO (Test Data Out) to TDI (Test Data In) ordering is required given the fact that IEEE 1149.1 is a serial protocol.

Because the DNX-50301 had three chains (one at 5 volts, and two at 3.3 volts), it was also necessary to draft up a small transceiver board that allowed all of the chains to be *externally* tied together at compatible voltage levels. Once we had our interface board, we tooled a fixture (see *Figure 5*) that allowed test probes to contact the JTAG signals of TDI, TDO, TMS, and TCK on all of the separate scan chains. To reconcile the modified netlist connectivity, it was a simple matter of re-defining the logical TDO to TDI ordering of the overall scan chain within the program.

Results:

We have put a total of 66 DNX-1U and 13 DNX-50301 boards through test. While troubleshooting is still an ongoing process, we have successfully repaired and shipped 57 boards to date (refer to Appendix A for detailed testing results). The ScanWorks test platform allowed us to interactively debug and diagnose failures that would normally only be detected on an in-circuit tester: open pins and traces, solder and copper shorts, defects under ball-grid ICs, and defective, wrong, or missing components. The boundary scan testing approach provided a mechanism to actively control signal levels *independent* of system clocking for purposes of debugging: this functionality is an extremely powerful feature of the system.

Conclusions:

While we have had positive results from our first test cases, test engineers should note two key limitations and requirements of boundary scan testing.

- First and foremost, boundary scan is not a replacement for good troubleshooting skills. Rather, it is a powerful tool that engineers and technicians can use to supplement conventional troubleshooting techniques.

- Second, boundary-scan testing applies only to boards that have incorporated boundary scan devices with a net count high enough to justify test development.

We developed case studies to evaluate the ASSET Boundary Scan Test Development System. First we evaluated the test capabilities of the system, and then we evaluated the comparative costs of boundary scan testing versus conventional troubleshooting. The results were straightforward: the tool is very effective and has been proven to save money, time, and company resources.

Appendix A: Troubleshooting Results

Serial #	Problem Found	Repaired	Shipped	Status	T/S Time	Location	DEF1	DEF2
BH0121	Reprog cpld, flash	**Y**	**Y**		10	U3,U13	PR	PR
BH0154	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH0165	Dead. U13 off 180deg, R135 open	**Y**	**Y**		20	U13,R135	OP	NS
BH0180	No boot-- open trace on U13.12 to R3	**Y**	**Y**		30	PCB	OP	
BH0195	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH0248	No scan; change U26	**Y**	**Y**		20	U26	BA	
BH0276	NDF			**In Rework**	15			
BH0278	Flash dead; intermittent open on watchdog	**Y**	**Y**		25	U3,U13	PR	PR
BH0322	NDF; change U7	**Y**	**Y**		15	U7	BA	
BH0336	Ethernet failure; no scannable component; NDF			**In Rework**	15			
BH0498	RESET/GND short; change U9			**In Rework**	25	U9	SH	
BH0511	Replace U26			**In Rework**	20	U26	BA	
BH0514	Watchdog resetting; change U1	**Y**	**Y**		20	U1	BA	
BH0559	LS1_RXDAT, LS1 _RXSIG stuck high			**In Rework**	20	LS1_RXDAT, LS1 _RXSIG	OP	
BH0697	U26 scan chain open; change U26; SS on U42	**Y**	**Y**		15	U26	PF	OP
BH0765	NDF			**In Rework**	15			
BH0795	Replace U3;resetting	**Y**	**Y**		30	U3	BA	
BH0798	Resetting; replace U3	**Y**	**Y**		20	U3	BA	
BH0838	OE in high frequency oscillation; wont program U3; change U3	**Y**	**Y**		25	U3	BA	
BH0875	U26.L17 open; SS via 1751, via 2994	**Y**	**Y**		75	U26.L17, VIA1751-2994	OP	SS
BH0884	U26-B22, C22 open			**In Rework**	15	U26.B22, C22	OP	
BH0921	Short-- BUF_ADR10,11	**Y**	**Y**		45	BUF_ADR10,11(U26)	SH	
BH1002	Flash won't erase; change U13	**Y**	**Y**		20	U13,R135	BA	
BH1211	HSSync Failure; replace U16,U17; R42 missing	**Y**	**Y**		20	U16,U17,R42	BA	BA
BH1215	Replace U26	**Y**	**Y**		20	U26	BA	
BH1278	HS Port failure at speed; replace U26			**In Rework**	25	U26	BA	
BH1342	Replace U26	**Y**	**Y**		20	U26	BA	
BH1367	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH1369	Reprog cpld, flash; fails after retest; replace U3 and U13			**In Rework**	20	U3,U13	BA	BA
BH1505	U3 decoder lines bad; replace U3	**Y**	**Y**		20	U3	BA	
BH1526	U26.D20 open-- R72 missing	**Y**	**Y**		15	U26.D20,R72	OP	MS
BH1527	U7, U10, U12 changed	**Y**	**Y**		20	U7,U10,U12	BA	BA
BH1572	U3 failed scan; reprog U3; reprog flas	**Y**	**Y**		25	U3,U13	PR	PR
BH1572	U3 failed scan; reprog U3; reprog flash	**Y**	**Y**		20	U3,U13	PR	PR
BH1643	U3 failed scan; reprog U3; reprog flas	**Y**	**Y**		30	U3,U13	PR	PR
BH1643	U3 failed scan; reprog U3; reprog flash	**Y**	**Y**		20	U3,U13	PR	PR
BH1775	U26.D20 open-- R72 missing	**Y**	**Y**		20	U26.D20,R72	OP	MS
BH1884	U26 scan chain open; change U26	**Y**	**Y**		15	U26	BA	
BH1894	SS on U3.19, SS VCC-GND			**SCRAP**	45	U3.19,VCC	SH	
BH1897	Replace U26	**Y**	**Y**		20	U26	BA	
BH1899	Reprog cpld, flash	**Y**	**Y**		15	U3,U13	BA	

BH1902	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH1979	CHS1and HS1_DTR stuck high			**In Rework**	20	CHS1and HS1_DTR	SH	
BH2154	Craft failure, PCB short			**In Rework**	20	PCB	SH	
BH2167	U3 dead; change U3	**Y**	**Y**		20	U3,U13	PR	PR
BH2231	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH2232	Via 2490 shorted to trace(nets QTIB_NIB1 to QTIB_HS)	**Y**	**Y**		15	Via2490	SS	
BH2330	NDF			**In Rework**	15			
BH2704	SS on BUF_ADR04, 05; U3 internal short; fails DRAM	**Y**	**Y**		15	BUF_ADR04-05,U3	SS	BA
BH2708	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH2750	NDF; ron found SS	**Y**	**Y**		20	R4	SS	
BH2926	U26-D20 open; second run U26 dead			**In Rework**	40	U26.D20	OP	
BH2936	U32 missing; reprog cpld, flash	**Y**	**Y**		25	U32	MS	
BH3020	Reprog cpld, flash	**Y**	**Y**		15	U3,U13	PR	PR
BH3028	Reprog cpld, flash	**Y**	**Y**		20	U3,U13	PR	PR
BH3122	Flash won't erase; change U13	**Y**	**Y**		70	U13	BA	
BH3174	Reprog cpld, flash	**Y**	**Y**		15	U3,U13	PR	PR
TH0104	No boot; open trace on net /DS; checked full net; XRAY	**Y**	**Y**		40	/DS	OP	
TH0119	NDF			**In Rework**	15			
TH0131	Replace U1; strobe on \RESET	**Y**	**Y**		30	U1	BA	
TH0132	NDF			**In Rework**	30			
TH0232	Failed contacts-- change U38	**Y**	**Y**		20	U38	BA	
TH0239	No boot-- SS; Failed ethernet-- change U31	**Y**	**Y**		30	U3.19-20,U31	SS	BA
TH0306	Failed contacts-- change U38	**Y**	**Y**		15	U38	BA	
TH0326	Failed ethernet-- change U31	**Y**	**Y**		20	U31	BA	
TH0333	U33 backwards	**Y**	**Y**		15	U33	BW	
Totals:	**Total Boards = 66**	**Repaired =50**	**Shipped =50**	**Rework=15**	**1510**	**23**	**Minutes per assy**	
				SCRAP=1	**25.17**	**Hours for 50 Assemblies**		

Test Engineer did ASSET testing / troubleshooting to validate system ($75/hour)

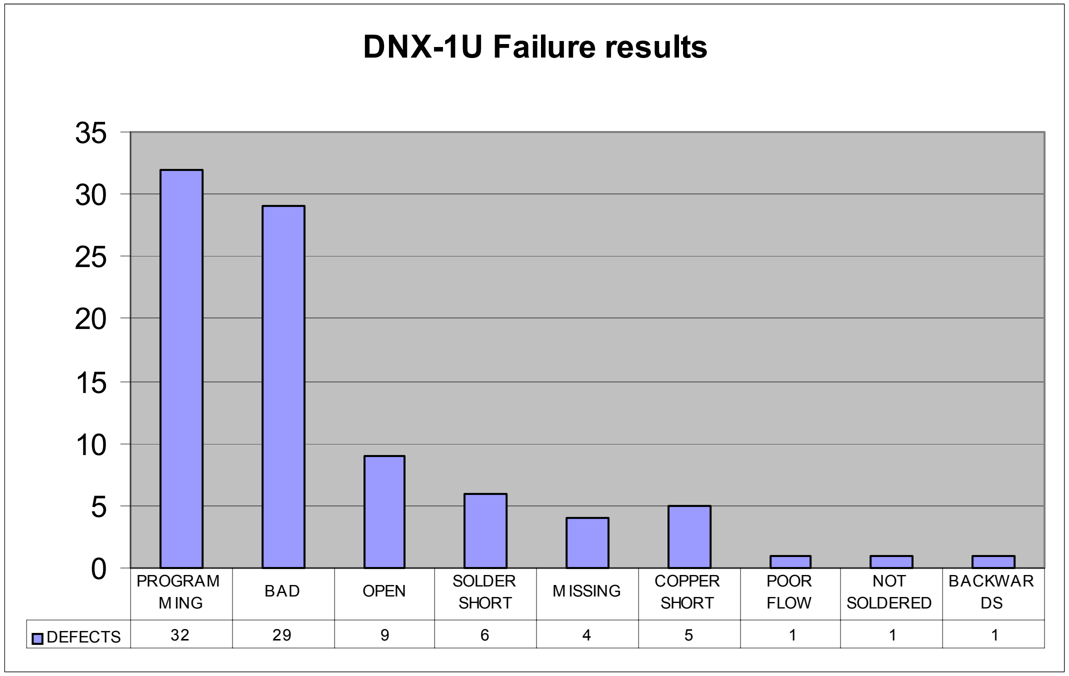
Actual Hours with ASSET system	25.17	Hours	$1,887.50	$38.52	TS cost per assembly with ASSET
Estimated Hours before ASSET System	396	Hours	$29,700.00	$606.12	est. TS cost per assembly without ASSET

Disposition of 51 Assemblies:		**Sell Price**
Repaired	**50**	**$75,000.00**
Shipped	**50**	**$75,000.00**
Still in Rework	**15**	**$22,500.00**
NCM (need decision on open trace repair)	**0**	**$0.00**
Scrap	**1**	**$1,500.00**

ASSEMBLY: DNX1U

$567.60	Savings per Assy
$27,812.50	Total est savings for 66 Assemblies

DEFECT	QUANTITY
PROGRAMMING	32
BAD	29
OPEN	9
SOLDER SHORT	6
MISSING	4
COPPER SHORT	5
POOR FLOW	1
NOT SOLDERED	1
BACKWARDS	1



Serial #	Problem Found	Repaired	Shipped	Status	T/S Time	Location	DEF1	DEF2	DEF 3
H49331	NDF			In Rework					
H50493	U37 dead	Y	Y		25	U37	BA		
H50494	NDF			In Rework					
H53514	U56 3.3V part; supposed to run at 5V	Y	Y		75	U56	WR		
H53516	U56 3.3V part; supposed to run at 5V	Y	Y		15	U56	WR		
H53517	U56 3.3V part; supposed to run at 5V	Y	Y		15	U56	WR		
H53518	U56 3.3V part; supposed to run at 5V	Y	Y		15	U56	WR		
H53523	1.8V rail dead	Y	Y		40	U65	BA		
H53533	NDF			In Rework					
H75874	NDF			In Rework					
H77026	NDF			In Rework					
H78373	Short SXILINX_Done to 3.3V	Y	Y		25	U29	SS		
Totals:	Total Boards = 13	Repaired =7	Shipped=7	Rework=5	210	30	Minutes per assy		
				SCRAP=0	3.50	Hours for 5 Assemblies			

Test Engineer did ASSET testing / troubleshooting to validate system ($75/hour)						
Actual Hours with ASSET system	3.50	Hours	$262.50	$5.36	TS cost per assembly with ASSET	
Estimated Hours before ASSET System	42	Hours	$3,150.00	$630.00	est. TS cost per assembly without ASSET	

Disposition of 51 Assemblies:		Sell Price
Repaired	7	$17,500.00
Shipped	7	$17,500.00
Still in Rework	5	$12,500.00
NCM (need decision on open trace repair)	0	$0.00
Scrap	0	$0.00

ASSEMBLY: 50301

$624.64	Savings per Assy
$2,887.50	Total est savings for 66 Assemblies

DEFECT	QUANTITY
WRONG PART	4
BAD PART	2
SOLDER SHORT	1